DESIGN AND SIMULATION OF TWO AND THREE-LEVEL HIGH POWER ACTIVE POWER FILTERS

A Thesis Submitted

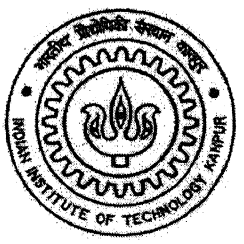
In partial Fulfillment of the Requirements

For the Degree of

Masters of Technology

By

Tefera Abate



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CERTIFICATE

It is certified that the work contained in this thesis entitled "*Design and Simulation of Two and Three-Level High Power Active Power Filters*", by Tefera Abate, has been carried out under my supervision and that this work has not been submitted elsewhere for any degree.

13/7/04

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Abstract

The importance of reactive power compensation and harmonic elimination is well known. In this thesis, reactive power compensation and harmonic elimination for high power application have been addressed. The high power active power filter (APF), which is used for load reactive and harmonic compensation, consists of two converters connected in parallel, namely, the main converter and the auxiliary converter. The main converter is a VSI with high power low frequency devices such as GTO, and is used to compensate for bulk amount of load reactive power. Two Level and Three Level Neutral point Clamped topologies are used in the main converter separately for comparison purposes. The gating signals for the main converter are generated in single-pulse as well multi-pulse PWM.

The auxiliary converter is a current controlled converter with low power high frequency devices, such as IGBT. The auxiliary converter compensates for load harmonics and the harmonics generated by the main converter.

An extensive simulation is carried out using PSCAD software package to ascertain the effectiveness of the scheme. Simulation results are presented to validate the proposed topologies.

Key words: Parallel converters, High power active power filters, Two and three-level converters

Contents

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

α	firing angle
C	capacitor
δ	phase shift angle
D1-D6	anti-parallel diodes of main converter
Da1-Da6	anti-parallel diodes of auxiliary converter
Ds1-Ds6	clamping diodes
iL	phase current through TCR
ILF(α)	magnitude of fundamental current of converter output
ILn(α)	magnitude of nth harmonic component of converter
Idc	DC current
I load	load current
Imain	main converter current
Iaux	auxiliary current
Icm1	fundamental component of main converter
Isref	source reference current
Imp	active component current
Imq	reactive component current
ImqL	load reactive current component
ImqC	converter reactive current component
Kf	ratio of vdcmin to Vdcaverage
L	inductor
Lm	main converter tie reactor
Laux	auxiliary converter tie reactor
Q	var supplied by compensator
S1-S6	main switches of the main converter
S1'-S6'	auxiliary switches of the main converter
Sa1-Sa6	switches of the auxiliary converter
Vsa,Vsb,Vsc	source voltages of phases a, b, and c respectively

Vdc	DC link voltage
Vdcmax	maximum dc link voltage
Vdcaverage	average dc link voltage
Vdcmin	minimum dc link voltage
v(t)	bus voltage at TCR and TSC
Xs	tie reactor
ω	utility frequency
Zmain	impedance between converter and coupling point

CHAPTER 1

Introduction

1.1 General

Power electronics is playing an important role in transmission and utilization of electrical power due to its capability of maintaining high efficiency and flexibility in the control process. The advent of modern self-commutated devices like GTOs, IGBTs and MCTs has further reinforced the utility of power electronic converters. However, the non-linear switching action of these devices gives rise to large reactive power demand and injection of harmonics into the utility.

Drawing of large VAR from the utility leads to:

1. Increased transmission and distribution losses, which results in under utilization of installed capacity.
2. Voltage drops at various buses and instability arising out of it. This also creates interferences amongst different loads connected to a bus.

Injection of harmonics in to the utility has also the following problems:

1. Increased loss in the equipments such as transformers and motors connected to the utility, and losses in conductors and cables.
2. Creates potential resonant conditions along with the capacitors present in the utility.
3. Saturation in transformers.
4. Malfunctioning of electronic circuit interfaced with the utility and disturbances in communication networks.

The negative impacts of reactive power and harmonics in the overall efficiency of the power systems, forced researchers to evolve various techniques of reactive power compensation and harmonics elimination.

The classical control methods of VAR compensation rely on the VAR generated or absorbed by the passive elements having energy storage capability. Since the VAR generated or absorbed is directly proportional to the energy storage capability of the passive elements, there is a considerable increase in the size of these elements with the increment in VAR to be compensated.

In the modern VAR compensators, the basic philosophy is to use the non-linear characteristics of power electronic switching in VAR generation and harmonic suppression. Theoretically as no energy storage passive elements are required, there is a significant reduction in size and projected cost of these classes of compensators. This results in low system losses and higher efficiency. It is worth mentioning here that, the VAR generating capability of this class of compensators is independent of the voltage prevailing at the point where they are connected. They also give a better flexibility in VAR management. Viability of this technology is ascertained in many research works and practical applications.

Active solutions to VAR compensation and harmonic elimination are, therefore, preferred to passive filter solutions. But, the long tail current associated with the power semiconductor devices characteristics prohibits high switching frequency operation at high power. Also, at high power, the efficiency of Active Power Filters (APF) is less due to significant switching loss. Therefore, good current control in high power application is not easy. To solve this problem, a new technique by combining high power low frequency devices and low lower high frequency devices has been reported to extract superior performance in VAR compensation [1, 2]. A high power converter (main converter), which consists of high power low frequency devices, is operated at low frequency, to deliver the VAR requirement of the load. Another converter (auxiliary converter), which consists of low power high frequency devices, is devoted for harmonic elimination, and is connected in parallel to it. Frequency of the main converter switches used in [1] was 650Hz. In [2] the frequency is reduced to the system power frequency, which further reduces switching losses implemented by single pulse width modulation.

1.2 Objectives

The advantages of active solution to VAR compensation over the passive solution have already been stated. Problems related to switching device characteristic put a serious limitation on the active solutions, especially in high power applications. The need for further improvement in the active solution has been met considering different control strategies and different topologies. In this thesis, High power active power filters have been proposed to fulfill the need for reactive power compensation and harmonic suppression. A parallel combination of high power low frequency (main) and low power high frequency (auxiliary) converters devoted for VAR compensation and harmonic suppression respectively has been used. The specific objectives of the thesis are (a) to design, analyze and simulate this parallel combination arrangement in two and three level VSI topologies for both linear and non linear loads (b) to make a performance comparison of the overall system while using single pulse and multi pulse based SPWM techniques for the generation of the main converter firing pulses.
Extensive simulation study using PSCAD is carried out to ascertain the effectiveness of the scheme.

1. 3 Literature Review

A lot of literature is available in the areas of reactive power compensation and harmonic elimination. The improvements made in the consecutive techniques also show us the effort towards more effective methods and encourage fellow researchers to evolve better topologies.

1.3.1 Classical VAR Compensators

1.3.1.1 Bank of Capacitors

Such capacitors are generally designed for compensating parameters that vary slowly, and the capacitors are usually fractioned so as to adjust the reactive power to be compensated [3].

Since the capacitors are elements that have discrete values, the techniques for shunt compensation may not allow the rapid variation in the reactive power to be followed.

1.3.1.2 Thyristor–Switched Capacitor (TSC)

These types of compensators involve capacitors switching by using bidirectional static switches and a small surge current limiting reactor in series, as shown in Fig. 1.1. But this type of switching will be possible only for a maximum value of supply voltage, which makes the waveform of the current sinusoidal at half the period at steady state [3]. This means that the capacitors should be kept at maximum voltage level obtained when the current goes to zero.

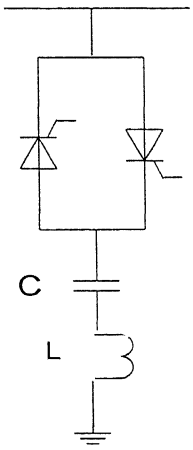

Fig. 1.1 Thyristor switched capacitor

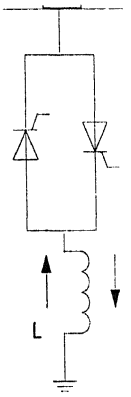

Fig. 1.2 Thyristor controlled reactor

Under steady state conditions, when the thyristor valve is closed, the TSC branch is connected to a sinusoidal ac voltage source, v = V sin(wt), and the current in the branch is given by [3]:

$$i(wt) = V\frac{n^2}{n^2-1}wC\cos wt$$

$$where \qquad (1.1)$$

$$n = \frac{1}{\sqrt{w^2LC}} = \sqrt{\frac{X_C}{X_L}}$$

The TSC may be commutated at zero voltage through the commutating of the thyristors and switched off when the current goes to zero. This type of control may be slow, since equating the supply capacitors voltages will lead to a delay in the action.

1.3.1.3 Thyristor Controlled Reactor (TCR)

This type of compensator is made up of an inductance supplied through an ac-ac converter made of two thyristors in anti-parallel as shown in Fig 1.2. The TCR current is always inductive; it absorbs only reactive power.

TCR is having considerable importance in an application area of power electronics that is commonly described as Static VAR compensation. In AC power networks, lagging reactive currents are undesirable because they cause excessive voltage drops and adversely affect the stability. Therefore, steps are taken to compensate for lagging reactive currents. In such schemes, Thyristor controlled reactors are commonly used in a manner explained below.

The current in the reactor can be controlled from maximum (Thyristor valve closed) to zero (Thyristor open) by the method of firing delay angle control, i.e, the closer of the thyristor valve is delayed with respect to the peak of the applied voltage in each half cycle, and thus the duration of the current conduction intervals is controlled.

With v(t) = V Cos(wt), the inductor current is given by [3]:

$$i_L(t) = \frac{1}{L}\int_{\alpha}^{wt} v(t)dt = \frac{V}{wL}(\sin wt - \sin\alpha) \qquad (1.2)$$

Since the Thyristor valve opens as the current reaches zero, the above equation is valid for the interval $\alpha \leq wt \leq \pi - \alpha$

For subsequent positive half cycles intervals the same expression remains valid.

The amplitude I_{LF} (a) of the fundamental reactor current i_{LF} (α) can be expressed as a function of α.

$$I_{LF}(\alpha) = \frac{V}{wL}(1 - \frac{2}{\pi}\alpha - \frac{1}{\pi}\sin 2\alpha) \qquad (1.3)$$

From equation 1.3 it is evident that the TCR can control the fundamental current from Zero to a maximum as if it as a variable reactive admittance. Thus, an effective reactive admittance, $B_L(\alpha)$, for the TCR can be defined.

$$BL(\alpha) = \frac{1}{wL}(1 - \frac{2}{\pi}\alpha - \frac{1}{\pi}\sin 2\alpha) \qquad (1.4)$$

If the TCR switching is restricted to a fixed delay angle, it becomes a Thyristor switched reactor (TSR). The TSR provides a fixed reactive current and it will be proportional to the applied voltage. Several TSRs can provide a reactive admittance controllable in a step like manner. If the TSRs are operated at $\alpha = 0$, the resultant steady state current will be sinusoidal.

The thyristor controlled reactor, in addition to the sinusoidal fundamental current, also generates harmonics. For identical positive and negative current half cycles, only odd harmonics are generated. The amplitudes of these are functions of the angle α, as expressed by the following equation:

$$I_{Ln}(\alpha) = \frac{V}{wL}\frac{4}{\pi}\left\{\frac{\sin\alpha\cos(n\alpha) - n\cos\alpha\sin(n\alpha)}{n(n^2-1)}\right\} \qquad (1.5)$$

Where n=2k+1, k=1, 2, 3.....

In a three-phase system, three single-phase Thyristor controlled reactors are used usually in delta connection. Under balanced load conditions, the triple-n harmonic currents circulate in the delta connected TCRs and do not enter the power system. The other harmonics generated by the TCRs can be reduced by various methods. One method,

particularly for high power applications, is to employ m parallel connected TCRs, each with 1/m of the total rating required (m>=2).

1.3.1.4 TSC and TCR Combination

Figure 1.3 shows the typical method of static VAR compensation.

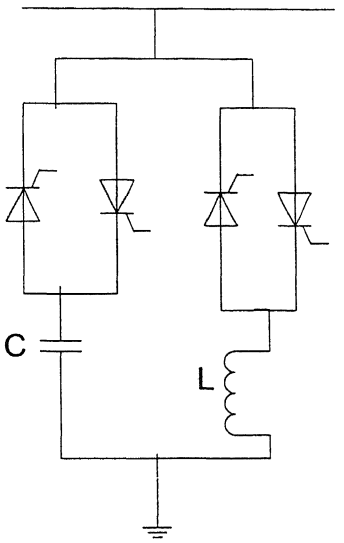

Fig. 1.3 Parallel combination of TSC and TCR

The leading reactive current necessary for VAR compensation is actually supplied by connecting capacitor banks across the ac lines. Here, the electromechanical breakers are replaced by thyristor valves. The problem faced, when connecting the capacitor to the high voltage lines, is the large inrush current that flows at the moment of contact if there is a large instantaneous voltage difference between the line and the capacitor. It is relatively easy to overcome this difficulty, because in addition to the series connected current limiter reactor the TSC uses static thyristor switches that can be gated at any desired instant in an ac cycle by means of a switching controller that will sense the voltage difference and gate the Thyristor at the correct instant in the ac cycle when the voltage difference is within permissible limits.

If only TSCs are employed for VAR compensation, the leading VAR to be introduced can only be adjusted in steps, because the switching is to be done one capacitor bank at a time. For precise adjustment of VAR, as dictated by the system requirements, a continually variable feature is desirable. This is achieved by having a thyristor-controlled reactor in parallel with the capacitor bank. If the maximum lagging current drawn by the TCR is equal to the leading VAR of the capacitor, the two will cancel and the net reactive VA will be zero. From this point, the lagging VAR of the TCR can be progressively decreased by phase control, thereby increasing the net leading VAR. After the maximum is reached, a further increase can be made by switching in another capacitor bank. In this manner the TSCs provide VAR in steps, while the TCR will provide the continuous adjustment between steps. This scheme enables precise and fast automatic adjustment of VAR by means of closed loop control.

1.4 Modern VAR Compensators

In the modern VAR compensator and harmonic suppressors the voltage-sourced inverter is used as it is more popular, than the current sourced inverter and is the base of most FACTS controllers. Reasons behind the popularity of VSI are stated in [1, 3]. To mention few:

1. Current sourced converters require power semiconductors with bi-directional voltage blocking capability. The available high power semi conductors with gate turn of capability (GTOs and IGBTs) either cannot block reverse voltage at all or can only do it with detrimental effect on other important parameters (e.g. Increased conduction losses)
2. Practical current source termination of the converter dc terminals by a current charged reactor has higher loss than complementary voltage source termination by a voltage charged capacitor.
3. The current sourced converter requires a voltage source termination at ac terminals, usually in the form of a capacitive filter. The voltage sourced converter requires a current source termination at the ac terminals that is naturally provided by the leakage inductance of the coupling transformer.

4. The voltage source termination (i.e a large dc capacitor tends to provide an automatic protection of the semi conductor against transmission line voltage transients. Current sourced converters may require additional over voltage protection or higher voltage rating of the semiconductors. However, the current sourced converters has a major advantage over there voltage sourced counter part in that they are almost totally immune to terminal shorts due to there inherent output current limitation provided by the dc current source.

In VSI, unidirectional dc voltage of a dc capacitor is presented to the ac side as ac voltage through sequential switching of devices. Through appropriate converter topology, it is possible to vary the ac output voltage in magnitude and also in any phase relation ship to the ac system voltage. The power reversal involves reversal of current, not the voltage. When the storage capacity of the dc capacitor is small, and there is no other power source connected to it, the converter cannot supply or absorb real power for much more than a cycle. The ac output voltage is maintained at 90^0 with reference to the ac current, leading or lagging, and the converter is used to absorb or supply reactive power only.

Depending on the methods used for controlling the compensator current, the voltage sourced inverter is grouped in to two [4]. The first category is when the inverter current is controlled indirectly by varying the converter output voltage.

The operation principle is explained in Fig. 1.4 by using a combination of two converters

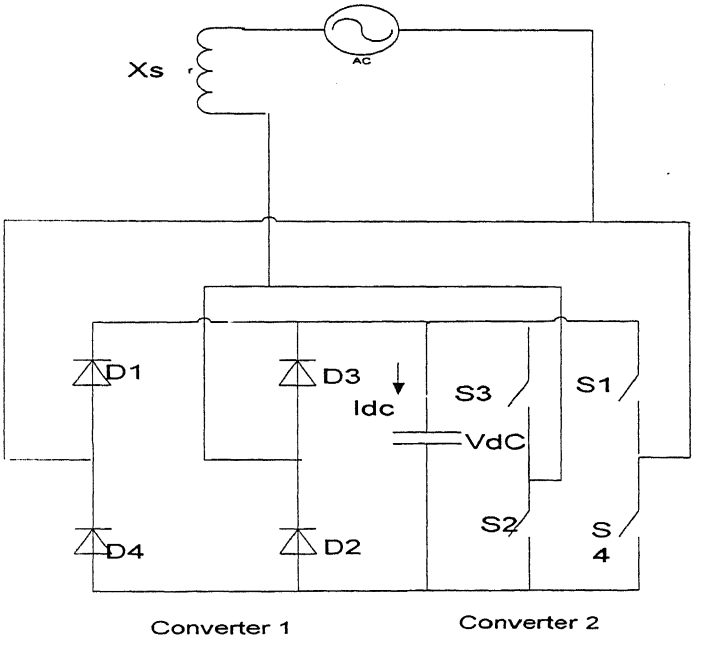

Fig. 1.4 Single phase voltage source converter

Converter i operates as uncontrolled rectifier through which a small quantity of real power flows from the ac side to the dc side, and converter 2 operates as an inverter when the real power flows in the reverse direction. Initially, when the converter 2 is not conducting, the capacitor C is charged up to the peak value of supply voltage through converter 1, and remains at this voltage for as long as there is no real power transfer between the circuit and the supply. If the switches of converter 2 are operated to obtain the fundamental of the converter output voltage slightly leading the ac main voltage, converter 2 conducts for a superior period to the one of the converter 1, causing a transfer of real power from the dc side to the ac side. In this way the dc capacitor voltage is decreased, and a reactive power is absorbed by the converter system (lagging mode).

The inverse is true when the fundamental of the converter output voltage slightly lags the supply voltage. The dc capacitor voltage is increased, and a reactive power is generated by the converter (leading mode). We can conclude that the reactive power, either generated or absorbed by the converter can be controlled only by one parameter: the phase angle between the converter output voltage and the supply voltage.

Thus as indicated by the phasor diagram shown in Fig. 1.5 when the amplitude of the inverter output voltage V_{oa} is smaller than the supply voltage V_{sa}, the reactive power is absorbed by the converter. Otherwise, the converter generates the reactive power when the amplitude of the supply voltage is larger than the output voltage of the inverter.

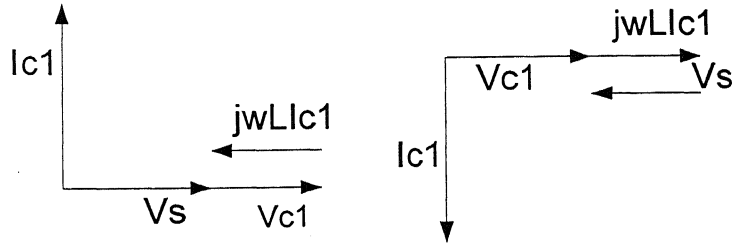

Fig. 1.5 Phasor diagram, leading and lagging current

The amount of reactive power supplied by the compensator is given by

$$Q = \frac{V_s |V_s - V_{c1}|}{\omega L} \tag{1.6}$$

The above equation shows that the converter can generate requisite VAR demand by controlling V_{c1} even if there is a variation in Vs. The phasor relationships modeling the loss component by R (shown in Fig. 1.7 for three phase), while supplying lagging and leading VAR are shown in (Fig 1.6).

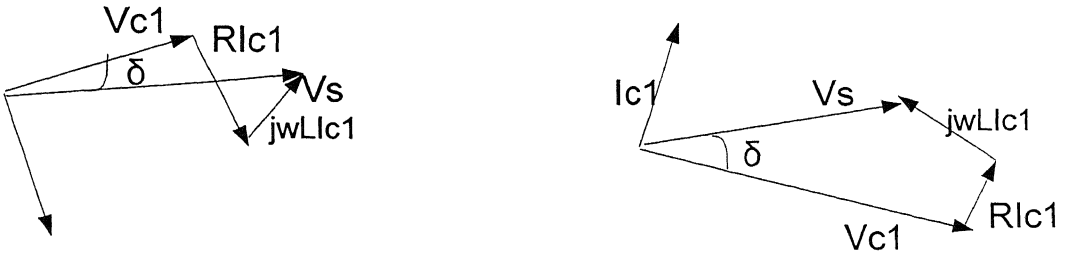

Fig. 1.6 Phasor diagram with the loss component considered

The same principle of operation is also applicable for three phase case, the power circuit configuration of which is shown in Fig. 1.7. The only difference between the two cases lies in the value of the dc link capacitance. Incase of three-phase system as the sum of the reactive volt amperes associated with the three phases at any instant is zero, theoretically the dc link voltage doesn't suffer from any distortion [3]. In single-phase topology the dc link voltage suffers a 2nd order harmonic distortion whose magnitude is proportional to Ic1. Thus to limit the dc link voltage ripple within acceptable margin of 10% of its average value, a fairly large capacitor is required for the single phase topology. Although the increment in capacitance of the electrolytic capacitor doesn't have a significant effect on the size and overall cost of the system, it degrades the dynamic performance of the compensation process.

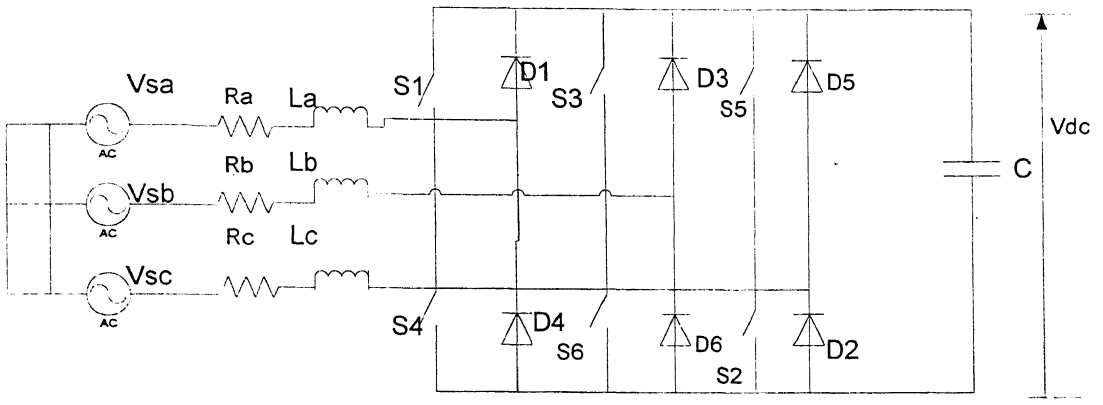

Fig. 1.7 Three phase voltage source converter

1.5 Control Strategy

VAR management by controlling Vdc is more popular. A scheme for load compensation, which ensures near unity power factor operation without sensing the load VAR demand is reported in [5]. By controlling the phase shift angle delta, the converter fundamental output voltage is made to equal the source voltage. With the increment in load, delta increases which results in the reduction of power factor. Thus by this technique complete compensation of the load VAR is not accomplished. Further, as the load is connected across the converter terminals, it gets contaminated by the harmonics present in the converter output voltages. In order to reduce these harmonics a passive filter is connected between the load and the converter terminals. This increases the passive component count and hence the size and cost of the system.

1.6 Reduction in Current Harmonics

Since the converter output voltage, V_c is generated by the virtue of non-linear switching action of the power devices; it is reach in harmonic content. Hence the compensator current, I_c also contains low order harmonics. A particular harmonic component, I_{cn} of the compensator current is given by

$$I_{cn} = \frac{V_{cn}}{nwL} \tag{1.7}$$

Where Vcn is the nth harmonic component of Vc. If the filter inductance, L is increased, the harmonic content of Ic can be reduced. But increment of L reduces the VAR rating capability of the compensator. Hence reduction in harmonics is not realized by increasing the filter inductor [1]. Harmonic reduction is generally accomplished by using PWM techniques for generating V_c. But these techniques wherein switching frequency is maintained high are suitable for low power applications. For high power applications due to switching frequency limitations for the high power devices, these PWM techniques can not be used. For these applications either parallel operated converter topology or multilevel converter topology is currently being used.[1,2].

1.7 Controlled Current Voltage Sourced VAR Compensator

The operating principle of these groups of converters is similar to that of controlled current AC-Dc synchronous converters [5]. Since the switching frequency of the devices for these types of converters is high, they are suitable for low to medium power applications in which BJTs, IGBTs, or MOSFETs are used as switching devices. This converter has superior current profile and good dynamic response compared to those of the indirect current controlled ones. Hence for low to medium power applications requiring fast compensating feature, the controlled current is a more viable solution.

The power circuit configuration of these compensators remains the same as that of the indirect current controlled ones. The power circuit of a single-phase topology is shown in Fig 1.8. A current reference I_{rfc} is generated and the compensator current, i_c is made to follow this reference within a hysteresis band. For increasing i_c, S4 and S3 are turned on while for decreasing S1 and S2 are turned on. DC link voltage, V_{dc}, is always maintained higher than the amplitude of V_s to ascertain current controllability at all operating points. Depending on the type of load compensated, i_{rfc} which is a sinusoid is made to lag or lead Vs by 90^0. As i_c is controlled to follow i_{rfc} within a small hysteresis band, it doesn't contain any low order harmonics. Reduction in the height of the hysteresis window improves the current harmonic spectrum but also increases the switching frequency. Thus

an optimum value for the window height should be chosen to obtain satisfactory current spectrum while keeping the switching frequency at a tolerable level. The same principle of operation is also valid for three-phase topology. Here three separate current reference, i_{rfca}, i_{rfcb} and i_{rfc} are generated for controlling three compensator phase currents, i_{ca}, i_{cb} and i_{cc}. In order to increase the current in a particular phase, the lower device associated with that phase is turned on while to decrease the current, the upper device is turned on.

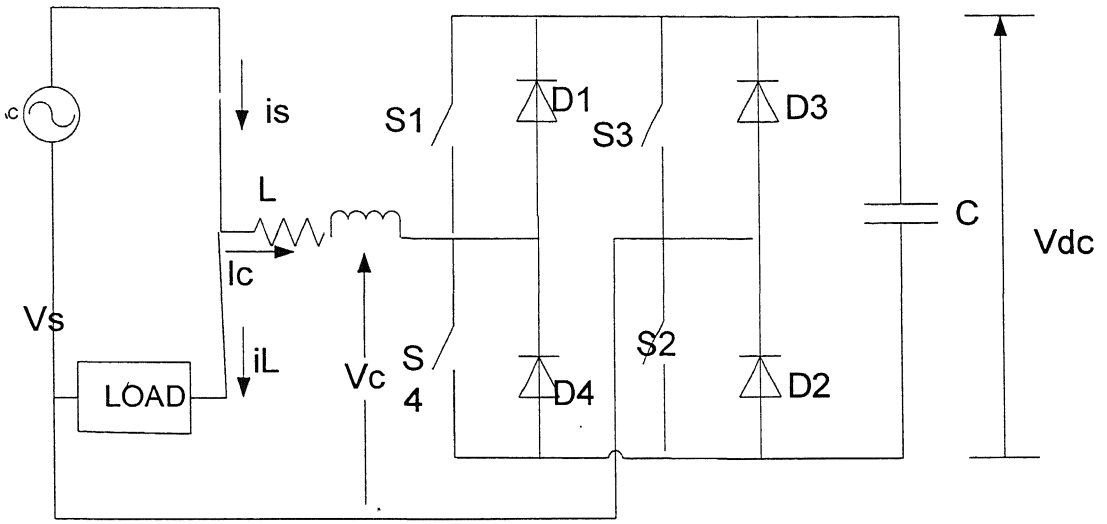

Fig. 1.8 Single phase controlled current VSI

1.8 Active Power Filter

When removal of load harmonics are desired from the controlled current converter, active power filter (APF) [1, 2] or active power line conditioner (APLC) [6] are used.

A scheme for high power VAR compensation and harmonic elimination is proposed in [1, 2]. The scheme comprised of high power low frequency VSI dedicated for VAR compensation (main converter) and a parallel connected low power high frequency, current controlled auxiliary converter devoted for harmonic elimination. In [1] the switching frequency of the main converter was 650 Hz, in [2] the switching frequency is further reduced to the line frequency, which helps in reducing the switching losses. In

both schemes, an SPWM technique is used to generate the firing pulses of the main converter. The error signal which is obtained as a difference of the main converter reactive current and the load reactive current, processed through a PI controller and acts as the information δ (for indirect current control) and modulating signals of the main converter are modified accordingly.

1.9 Conclusion

The review presented here confirms the attempts to improve the capabilities of compensators performance with the help of topological modifications, converter voltage waveforms, and harmonic elimination and control methodologies. It also reveals the inevitability of further modifications and performance improvements.

CHAPTER 2

Design and Simulation of Two Level Converter Based Active Power Filter (APF)

2.1 Power Circuit Configuration

A three phase, three wire star connected utility is considered. The combined active power filter is connected in parallel to the load. The main converter used here is a two level (six step) voltage source inverter (VSI), (Fig. 2.1) with high power low frequency devices. The auxiliary converter is connected in parallel with the main converter sharing the same dc link. Low power high frequency devices (IGBT) are used in the auxiliary converter [7].

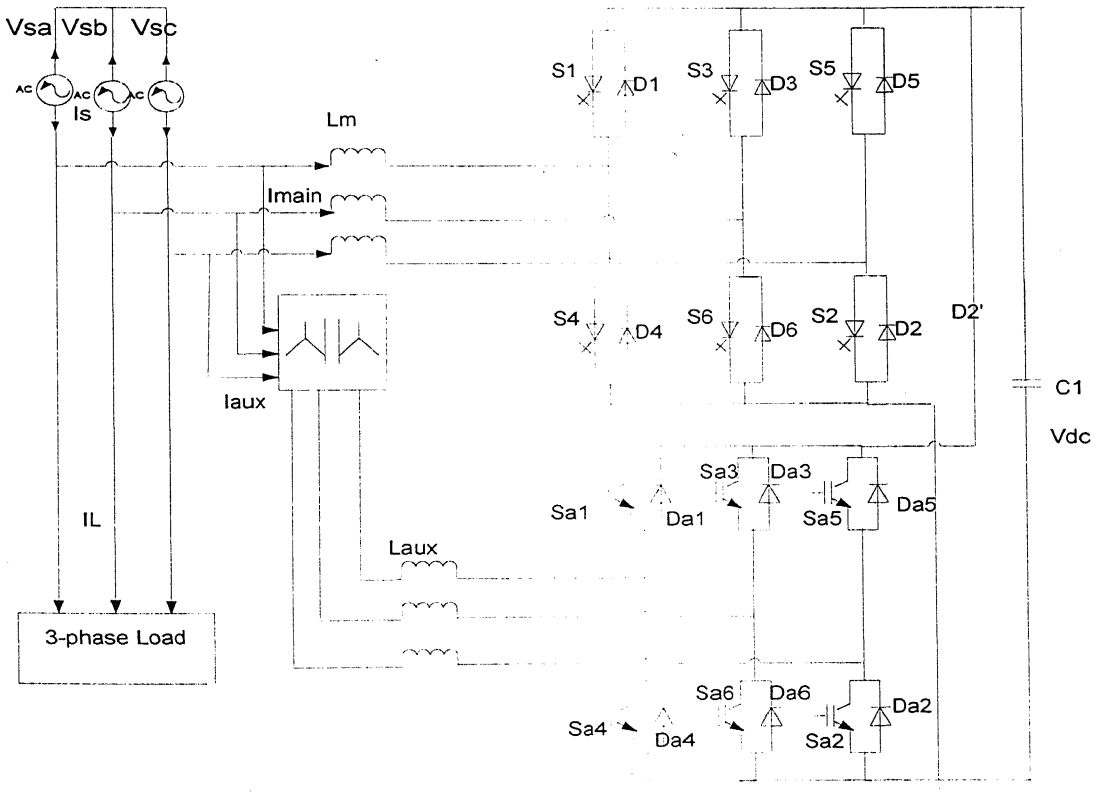

Fig. 2.1 Power circuit configuration of six-step APF

Both single pulse and multi pulse SPWM techniques are implemented for comparison purposes. In case of the single pulse, the switching frequency of the main converter devices is kept same as the utility frequency so that switching loss is minimized and the full utilization of the current carrying capability of switching devices is realized. In the multi-pulse SPWM case, a switching frequency of 600 Hz (three pulses per quarter cycle) is used. Thus, in both cases, the main converter can carry the high reactive power demand of the load.

The auxiliary converter consists of low power high frequency devices (IGBT) controlled by current controlled modulation technique. It eliminates the main converter current harmonics and the load current harmonics from flowing to the utility current by high switching frequency operation.

The two converters share the same dc-link capacitor leading to a compact structure. To avoid circulating currents between the two converters, the auxiliary converter is connected in parallel to the load as well as the main converter with an isolation transformer.

The effects on both linear and non-linear loads in both the single as well multi-pulse based SPWM have been studied. The non-linear load used here is a simple uncontrolled full bridge rectifier.

2.2 Basic Operating Principle of the VSI

The basic voltage sourced inverter scheme for reactive power generation is shown schematically in Fig. 2.2 [3].

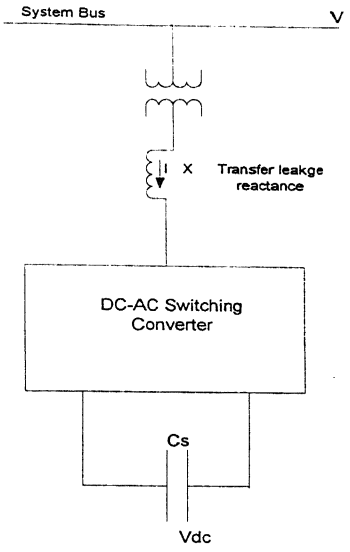

Fig. 2.2 Voltage sourced inverter

From a dc voltage source, as provided by the charged capacitor Cs, the converter produces a set of controllable three phase output voltages with the frequency of the ac power system. In ideal case, each output voltage is in phase with and coupled to the corresponding ac system voltage via a relatively small tie reactor (which in practice is provided by the per phase leakage inductance of the coupling transformers).

By varying the amplitude of the output voltage, the reactive power exchange between the converter and the ac system can be controlled in a manner similar to that of the rotating synchronous machine. That is, if the amplitude of the output voltage is increased above that of the ac system voltage, then the current flows through the tie reactance from the converter to the ac system and the converter generates reactive (capacitive) power for the ac system. If the amplitude of the output voltage is decreased below that of the ac system, then the reactive current flows from the ac system to the converter and the converter absorbs reactive (inductive) power. If the amplitude of the output voltage is equal to that of the ac system, the reactive power exchange will be zero.

In this thesis, the amplitude difference between the converter output voltage and the system voltage is achieved rather by varying the voltage of the capacitor Cs. This is achieved by controlling the phase angle (δ) between the utility voltage and the converter

output voltage. In the multi-pulse SPWM, the modulating signal is shifted by δ, so that the resulting firing pulses will also shift by δ. In the single pulse this is achieved by direct shifting of the entire pulse train.

In an ideal case, as the converter supplies only reactive output power, its output voltages are controlled in phase with the ac system voltage. The real input power provided by the dc source (charged capacitor) must be zero (as the total instantaneous power on the ac side is also zero). Furthermore, since reactive power at zero frequency (at the dc capacitor) by definition is zero, the dc capacitor plays no part in the reactive power generation. In other words, the converter simply interconnects the three ac thermals in such a way that the reactive output currents can flow freely between them [3]. Viewing this from the terminals of the ac system, one could say that the converter establishes a circulating current flow among the phases with zero net instantaneous power exchange.

The output voltage wave form of the dc to ac converter is not a perfect sine wave. For this reason, the net instantaneous output power (VA) has a fluctuating component even if the output currents are sine waves (which condition is approximated quite closely in practical systems). Thus in order not to violate the equality of instantaneous output and input powers, the converter must draw a fluctuating (ripple) current from the dc storage capacitor that provides a constant voltage termination at the input.

2.3 Design of DC Link Capacitor

The dc link capacitor is chosen to limit the ripple in the dc link voltage within a permissible limit. The limit is generally taken to be 10 % of the average dc link voltage . As this ripple is proportional to the amount of reactive volt ampere to be compensated, the value of the dc link capacitor is determined by the maximum VAR handled by the compensator [1]. In the present scheme, as the capacitor will have to supply or absorb load real power during transient period, the method followed for selecting the dc link capacitance is as follows:

The dc link voltage is sensed and compared with the reference dc-link voltage command V_{dcref} to control the amplitude of the reference current.

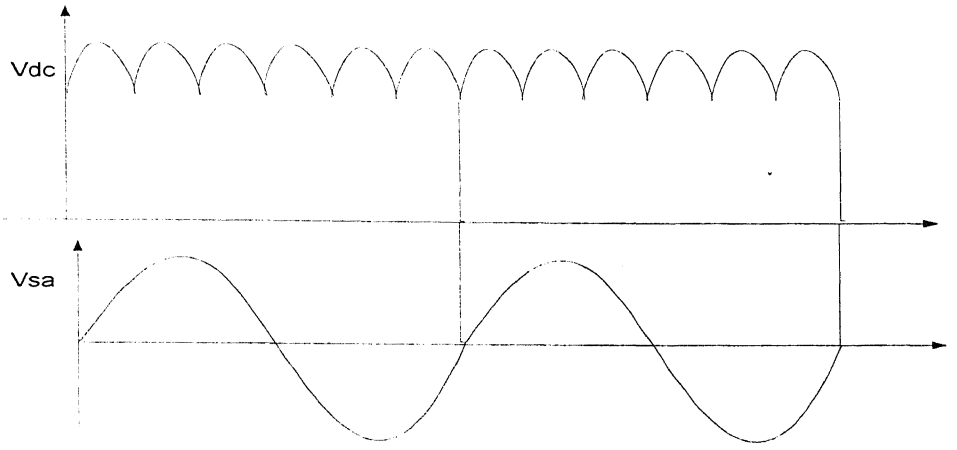

Fig. 2.3 DC- link voltage profile

It can be observed from the Figure that the magnitude of the capacitor voltage remains constant at all the zero crossing instants of the source voltage. If the dc voltage is sampled only at these instants, the reference current level set at the beginning of a cycle remains constant throughout the cycle.

Therefore, for controlling the reference source current in a discrete mode, the capacitor may have to supply or absorb the load real power for one cycle of the utility voltage during the worst case of transient. The worst case of transient is encountered when the real component of load current has changed from zero to its full load value and this change has occurred just after the beginning of the sampled cycle. Since the amplitude of reference source current is maintained at a value corresponding to zero active component of the load current, the capacitor has to supply the rated active component of the load for a full cycle of the utility. As a result, the dc link voltage decreases throughout this cycle. Hence the design guideline for the dc link capacitor should be such that even during the worst case of transient, the dc link voltage should not fall below the value required for source current controllability.

The average rate at which energy is being absorbed by the capacitor is given by:

$$p_{cap} = v_{dc} I_c$$

$$P_{cap} = v_{dc} C \frac{d}{dt} v_{dc}$$

$$\int P_{cap} dt = \int v_{dc} C dv_{dc} \qquad (2.1)$$

$$E\max = \frac{1}{2} C(v^2{}_{dc\max} - v^2{}_{dc\min})$$

With

$$q_{\max} = 3V_{\max} I_{\max q}$$

$$q_{\max} = V_{\max} I_{\max q} \quad \text{(in single phase basis)}$$

$$where\ I_{\max q} = \frac{V_{conv\max} - V_{pcc}}{x}$$

$$\Rightarrow V_{conv\max} = \frac{q_{\max} * x}{V_{pcc}} + V_{pcc}$$

$$but\ V_{conv\max} = \frac{4}{\pi}\left(\frac{V_{dc\max}}{2}\cos\alpha\right)$$

Fixing suitable value for V_{dcmax},

L can be computed using the following formula:

$$L = \left(\frac{V_{conv\max} - V_{pcc}}{q_{\max} * w}\right) V_{pcc}$$

Let the peak power rating of the load be P_{max} watt and the rms utility voltage be Vs volt. Therefore, the maximum energy that the capacitor has to supply in the worst case of transients given by:

$$E_{\max} = p_{\max} \times T \ \ [J] \qquad (2.2)$$

The dc link capacitor C is therefore, obtained by equating equations (2.1) and (2.2)

$$C = \frac{2 \times P_{\max} \times 20 \times 10^{-3}}{vdc^2 (1 - kf^2)} F$$

Where, as the ripple of dc voltage has to be maintained at 10%

$$v_{dc\max} = v_{dcaverage} + \frac{10}{100} v_{dcaverage}$$

$$v_{dc\min} = v_{dcaverage} - \frac{10}{100} v_{dcaverage}$$

$$kf = \frac{V_{dc\min}}{V_{dcaverage}}$$

The value of *kf* is judiciously chosen so that the source current controllability is ascertained at all operating points.

In this thesis, as the system voltage considered is 11 kV (L_L), taking the minimum dc voltage to be equal to a magnitude which result 11 kV (rms) fundamental at which the reactive power transfer will be zero (7.78 kV), P=20 MW, the capacitor value is calculated to be 6.5 mF with an assumed dc ripple voltage of 15% and a judiciously obtained kf of 0.85.

2.4 Control Strategy

A VSI, in general, comprises a large number of gate controlled semi-conductor power switches. The gating commands for these devices are generated by the internal converter control in response to the demand for reactive and/or real power reference signal(s). In this thesis as aforementioned, a comparison is made for the single pulse as well multi-pulse based SPWM. In case of single pulse, a 180^0 conduction is considered, and a total shifting of this pulse by an angle δ is used as a control strategy. In the multi-pulse based a simple selective harmonic elimination technique is implemented, and the 3^{rd} and 5^{th} harmonics are the current targets here to be eliminated.

With the method of *Selective Harmonic Elimination*, only selected harmonics are eliminated with the smallest number of switching. For a two level PWM waveform with odd and half wave symmetries and n chops per quarter cycle shown in Fig 2.4, the peak magnitude of the harmonic components including the fundamental, are given by (2.3).

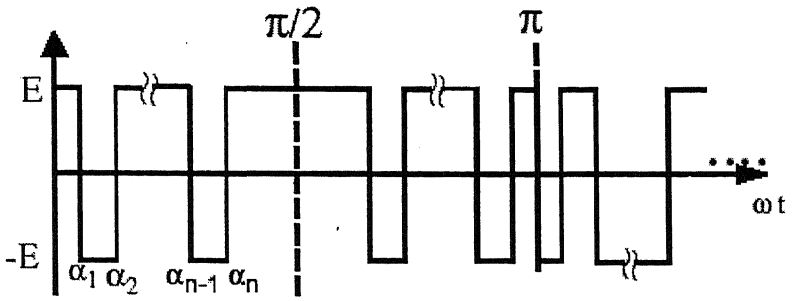

Fig. 2.4 A two-level PWM waveform with odd and half wave symm

$$h_1 = \left(4\frac{E}{\pi}\right)\left[1 - 2\cos\alpha_1 + 2\cos\alpha_2 - 2\cos\alpha_3 .....2\cos\alpha_n\right]$$

$$h_3 = \left(4\frac{E}{3\pi}\right)\left[1 - 2\cos\alpha_1 + 2\cos\alpha_2 - 2\cos\alpha_3 .....2\cos\alpha_n\right]$$

.

.

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$$h_k = \left(4\frac{E}{k\pi}\right)\left[1 - 2\cos\alpha_1 + 2\cos\alpha_2 - 2\cos\alpha_3 .....2\cos\alpha_n\right] \qquad (2.3)$$

Here h_i is the magnitude of the i^{th} harmonic and α_j is the j^{th} primary switching angle. Even harmonics do not show up because of the half-wave symmetry.

The n pulses in the waveform afford n degrees of freedom. Several control options are thus possible.

For example n selected harmonics can be eliminated. Another option which is used here is to eliminate n-1 selected harmonics and use the remaining degree of freedom to control the fundamental frequency ac voltage. To find the α_j 's required to achieve this objective, it is sufficient to set the corresponding h's in the above equations to the desired values (0 for the n-1 harmonics to be eliminated and the desired per-unit ac magnitude for the fundamental) and solve for the α_j's. Equation 2.2 can be readily proved by finding the Fourier coefficients of the waveform as shown in Fig. 2.4. In general, for a periodic waveform with period T, the Fourier Cosine and Sine Coefficients are given by:

$$a_0 = \frac{1}{2\pi}\int_0^{2\pi} f(\theta)\,d\theta$$

$$a_k = \frac{1}{\pi}\int_0^{2\pi} f(k\theta)\cos(k\theta)\,d\theta$$

$$b_k = \frac{1}{\pi}\int_0^{2\pi} f(k\theta)\sin(k\theta)\,d\theta$$

Because of the half-cycle symmetry of the waveform of Fig. 2.4, only odd order harmonics exist. Also, it is easy to see that the Fourier Cosine coefficients disappear with the choice of coordinate axes used. Utilizing the quarter cycle symmetry, the Fourier Sine coefficients become:

$$b_k = \frac{4}{\pi}\int_0^{2\pi} f(k\theta)\sin(k\theta)\,d\theta$$

Substituting the two-valued PWM waveform, one obtains (see Fig 2. 4):

$$b_n = \frac{4E}{\pi}\left(\int_0^{\alpha 1}\sin(k\theta)d\theta - \int_{\alpha 1}^{\alpha 2}\sin(k\theta)d\theta + \int_{\alpha 2}^{\alpha 3}\sin(k\theta)d\theta \ldots\ldots \int_{\alpha n}^{\frac{\pi}{2}}\sin(nk\theta)d\theta\right)$$

$$= \frac{4E}{k\pi}\left(-\cos(k\theta)\Big|_0^{\alpha_1} + \cos(k\theta)\Big|_{\alpha 1}^{\alpha 2} - \cos(k\theta)\Big|_{\alpha 2}^{\alpha 3} \ldots\ldots\right)$$

$$= \left(4\frac{E}{n\pi}\right)\left[1 - 2\cos n\alpha_1 + 2\cos k\alpha_2 - 2\cos k\alpha_3 \ldots..2\cos\alpha_n\right]$$

In this thesis, three pulses per quarter cycle, which allow for three degrees of freedom, are used. We may use these to eliminate two harmonics and control the magnitude of the fundamental to any desired value:

The Selective Harmonic Elimination (SHE) is applied with a view to controlling the fundamental component of voltage to a fixed magnitude equal to the system voltage, and eliminating the 3rd and 5th harmonics.

As three objectives are to be achieved, we need 3 chops. The fundamental, 3rd and 5th harmonic magnitudes are given by:

$$V_1 = \frac{4E}{\pi}(1 - 2\cos(\alpha_1) + 2\cos(\alpha_2) - 2\cos(\alpha_3))$$

$$V_3 = \frac{4E}{3\pi}(1 - 2\cos(3\alpha_1) + 2\cos(3\alpha_2) - 2\cos(3\alpha_3))$$

$$V_5 = \frac{4E}{5\pi}(1 - 2\cos(5\alpha_1) + 2\cos(5\alpha_2) - 2\cos(5\alpha_3))$$

It is required that

$$V_1 = 1 \text{ pu}$$

$$V_3 = 0$$

$$V_5 = 0$$

This gives us three equations in the three unknowns' α_1, α_2 and α_3. Solving numerically we get:

$$\alpha_1 = 27.432^0$$
$$\alpha_3 = 42.131^0$$
$$\alpha_5 = 85.62^0$$

These signals are then used as firing pulses for the main converter. The pulse angles are fixed in a cycle and the whole voltage waveform is shifted to realize the phase angle δ. The resulting converter output voltage is shown in Fig. 2.5 below

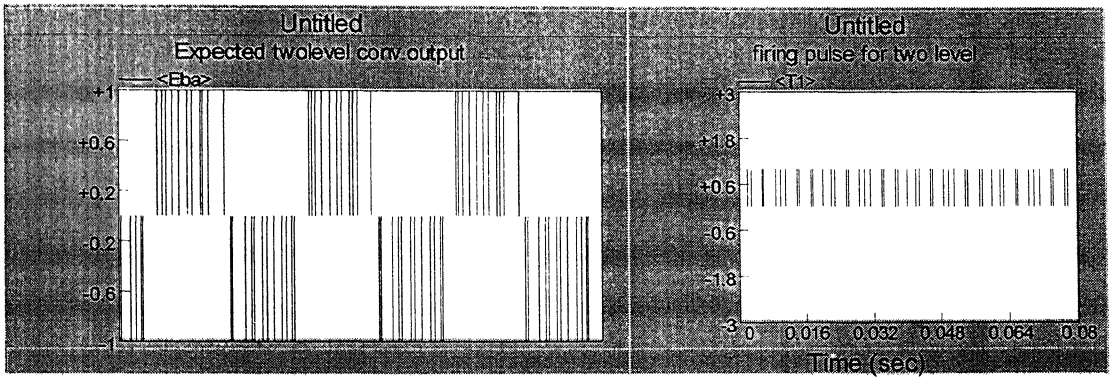


Fig. 2.5a. Expected converter output voltage b. Firing pulse with inverter logic used

In both single pulse as well multi-pulse based SPWM, the reference signals are provided by the external or system control, from the operator instructions and system variables, which determine the functional operation of the STATCOM.

The main function of the internal control is to operate the converter power switches so as to generate a fundamental output voltage waveform with the demanded magnitude and phase angle in synchronism with the ac system.

In this way the power converter with the internal control can be viewed as a sinusoidal, synchronous voltage sources behind a tie reactor (provided by the leakage inductance of the coupling transformers) the phase (in this approach) of which is controlled by the external control via appropriate reference signal(s) Fig. 2.6.

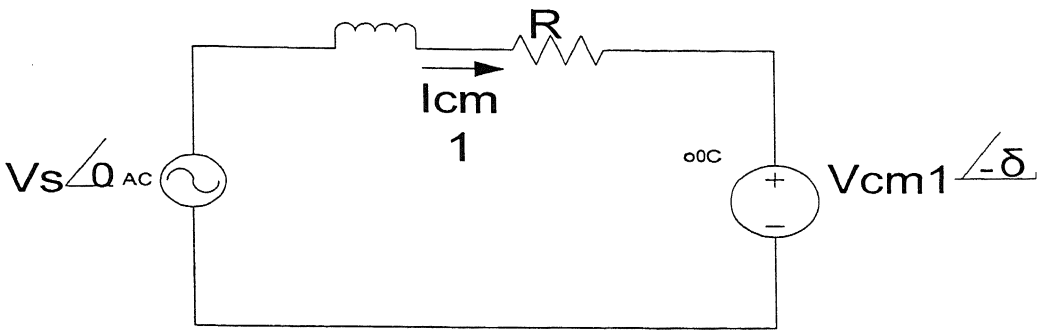


Fig. 2.6 Per-phase equivalent circuit of the main converter

Since the main converter is responsible to supply the fundamental VAR requirement of the load, the main converter current is compared with the fundamental reactive load current to generate the reactive power current error. The reactive current error is processed through a PI controller to control the voltage delay angle delta of the main converter as V_{cm1} for indirect current control. The change of delta leads to a change of active power flow between the utility and the main converter as V_{cm1} undergoes phase change relative to the system voltage. Hence, the main converter current in reference to Fig. 2.3 varies according to the following equation:

$$I_{cm1} = \frac{V_s - V_{cm1}\angle -\delta}{Z_{main}} \tag{2.4}$$

Where V_s is the supply voltage; Z_{main} is the impedance of the inductor connecting the main converter to the supply; I_{cm1} is the fundamental rms current of the main converter and V_{cm1} is the fundamental converter output voltage.

2.4.1 Determination of the Fundamental Output Voltage for Single Pulse PWM

Considering a 180^0 conduction, the output voltage waveform is shown in Fig. 2.7 below. Fourier analysis of output of two level converter gives the following results.

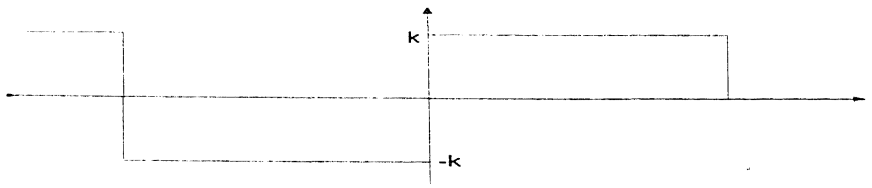


Fig. 2.7 Single pulse converter output voltage

$$f(x) = -k \quad for \quad -\pi < x < 0$$
$$= k \quad for \quad 0 < x < \pi$$
$$and \quad f(x + 2 * \pi) = f(x)$$

$$a_0 = \frac{1}{2 * \pi}\int_{-\pi}^{\pi} f(x)\,dx = \frac{1}{2 * \pi}\left[\int_{-\pi}^{0} -k\,dx + \int_{0}^{\pi} k\,dx\right]$$
$$= \frac{1}{2 * \pi}(0 - -k * (-\pi) + k\pi)$$
$$= 0$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x) * \cos nx\,dx = \frac{1}{\pi}\left[\int_{-\pi}^{0} -k\cos nx\,dx + \int_{0}^{x} k\cos nx\,dx\right]$$
$$= 0$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\sin xdx = \frac{1}{\pi}\left[\int_{-\pi}^{0} -k\sin nxdx + \int_{0}^{\pi} k\sin nxdx\right]$$
$$= \frac{2 * k}{n\pi}(1 - \cos n\pi)$$
$$\cos n\pi = -1 \quad for \quad odd \quad n$$
$$= 1 \quad for \quad even \quad n$$

therefore $1 - \cos n\pi = 2$ *for odd n and zero for even n* (2.5)

$$\Rightarrow b_1 = \frac{4k}{\pi};\quad b_3 = \frac{4k}{3\pi};\ b_5 = \frac{4k}{5\pi}$$

$$\therefore f(x) = \frac{4k}{n\pi}(\sin x + \sin 3x + \sin 5x + ...)$$

$$V_{cm1} = \sum_{n}^{\infty} \frac{4k}{n\pi}(V_{dc} \sin nwt) \quad for \quad n = odd$$

2.4.2 Estimation of Reference Current and Delta

The complete system control block diagram for the 6-step–APF is given in Fig. 2.8.

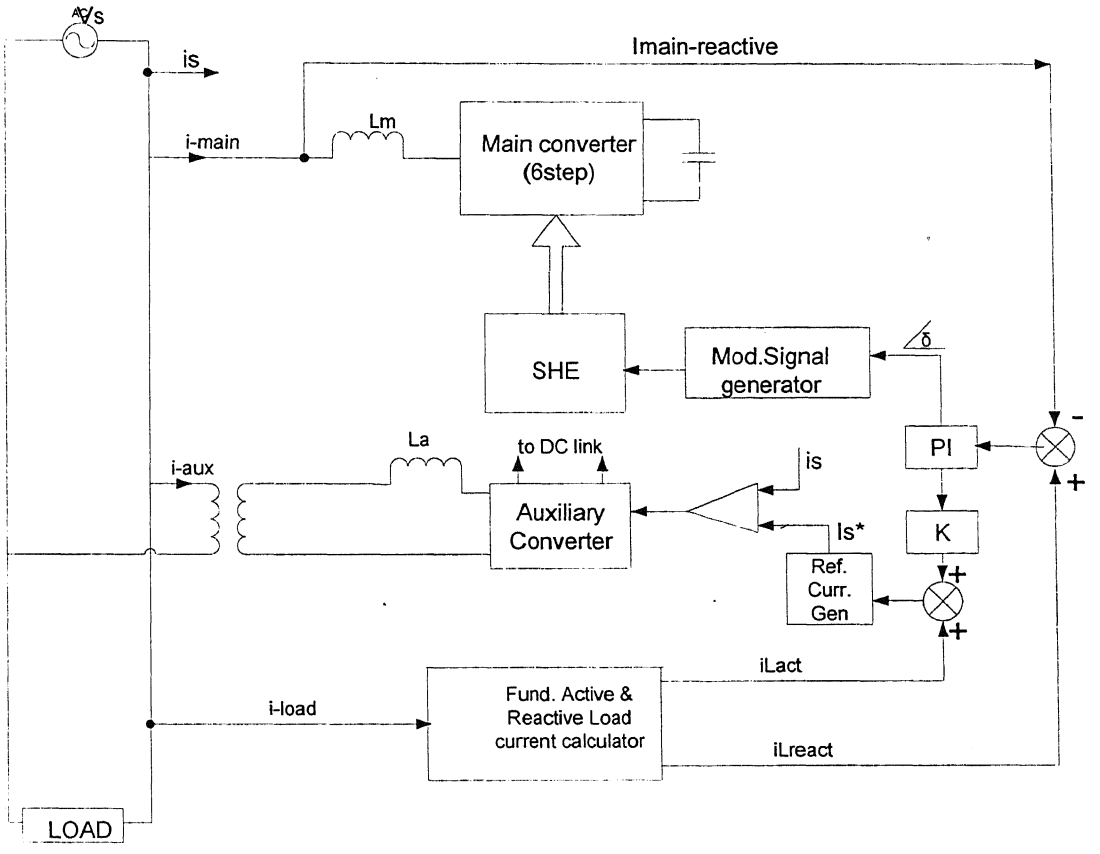


Fig 2.8 Control block diagram of the proposed 6-step converter based APF

As the ultimate goal is the reactive and harmonic current compensation, the utility should supply only the active component of load current and the loss component of the converter at unity power factor. Therefore, the supply current should be always in phase with the respective phase voltage.

The actual reactive current of the compensator is deducted from the load reactive current requirement, which can be referred to as the reactive reference current. The error signal is

processed through a PI controller and a limiter to generate the phase angle of the converter voltage, δ.

In ideal case, angle δ is supposed to be zero, as the main converter current provides only the load reactive current, which is at quadrature with the supply voltage. However, because of the converter losses, the capacitor voltage tends to fall and requires a small amount of active current from the supply to maintain the charge. So the angle δ acts as a measure of converter losses.

To determine the reference magnitude of the source current, a control signal proportional to δ is added with the active component of the load current I_{Lact}. This amplitude multiplied by a sine-template (in phase with the utility phase voltage) gives the reference utility current I_{sref} for the respective phase. These reference currents have to do with the auxiliary converter.

A sinusoidal reference current I_{sref} in phase with the utility voltage is synthesized and the source current I_s is forced to follow this reference with a hysteresis band. The source current is sensed and compared with the reference current. The error thus obtained decides the switching instants of the auxiliary compensator devices.

Current in each phase is controlled independently. In order to increase the current of a particular phase, lower devices of the auxiliary compensator associated with that phase, is turned on. While for decreasing the current, upper device associated with that particular phase is turned on. [7]

$$\begin{aligned} I_{ref} &= k \times \delta + I_{Lp} \\ Isref(a) &= I_{ref} \sin \omega t \\ Isref(b) &= I_{ref} \sin(\omega t - 120^{\circ}) \\ Isref(c) &= I_{ref} \sin(\omega t + 120^{\circ}) \end{aligned} \tag{2.6}$$

Where k is determined judiciously

The following approach is used to determine delta:

$$P = \frac{1}{T} \int vidt \tag{2.7}$$

$$let\ v_a = v\sin wt$$

And

$$va^I = v\sin(wt - \frac{\pi}{2})$$

$$\Rightarrow \frac{1}{T}\int v_a i_a dt = \frac{I_{mp}V_m}{2} \tag{2.8}$$

I_{mp} is the active current component

and $$\frac{1}{T}\int v_a^I i_a dt = \frac{I_{mq}V_m}{2} \tag{2.9}$$

Where I_{mq} is the reactive component of the current

Both the load and the converter reactive current components are taken this way, compared, processed by a PI controller and resulted delta as shown in Fig. 2.6

2.5 Simulation Results

The simulation study is carried out by using PSCAD software package. The ready-made function blocks available helped a lot in making ease of the construction of the overall circuit. The built in FORTRAN program gives a very good freedom to construct specifically required blocks in the domain of the thesis, like firing circuits for the main as well auxiliary converters.

The performance of the combined (main-auxiliary) converters in both single and multi pulse cases, is thoroughly studied and resulted waveforms are analyzed for the very best conclusion.

In general, for ease of comparison, the procedure followed in the presentation is as follows: a load of a given MVA is connected to the system voltage in parallel with the combined main-auxiliary converter.

Initially, only with the main converter being active, its effect on the system is studied.

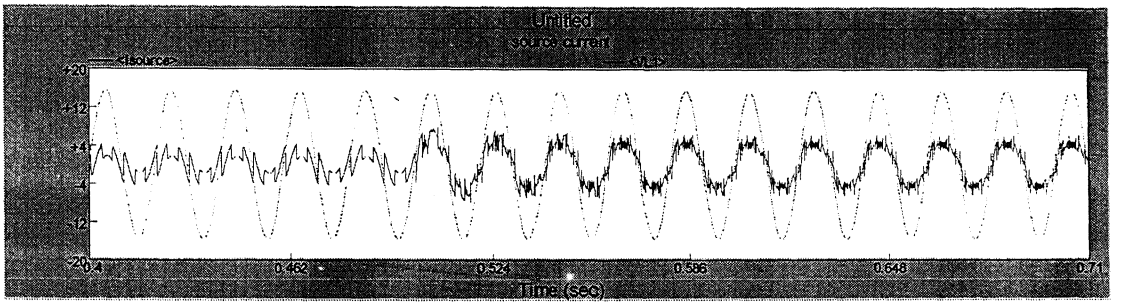
It is observed here the converter VAR building up and taking over the responsibility the source catering the reactive demand of the load from the source. With this condition, the harmonic content of the source current is analyzed. When the main converter current gets stable, the auxiliary converter is made on. Now it is logical and the right time for the

stable, the auxiliary converter is made on. Now it is logical and the right time for the question of the reduction of the harmonic level due to the auxiliary converter to come in to picture. Corresponding Figures are shown to respond for the question.
A detailed analysis, as to whether the harmonic level before turning on the auxiliary converter was un acceptable according to IEEE-519 Standard or not and whether the auxiliary converter made the harmonics to an acceptable level, is made graphically as well mathematically by using the harmonic spectrums and THD respectively.

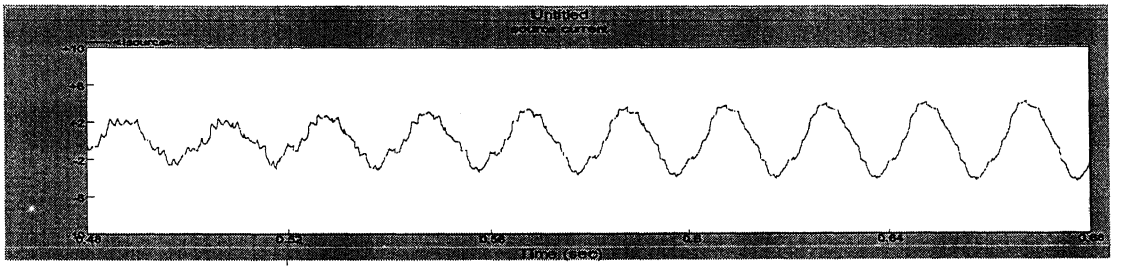
2.5.1 Performance of Single and Multi-Pulse Based Six-Step Converter for VAR Compensation of Linear Loads

A three phase star connected 40 MVA linear load is considered in a 7.78 kV rms. Three phase three wire system is considered. For comparison purposes, results obtained from both cases (by which firing pulse generation for the main converter is made by use of single pulse and multi pulse SPWM) are given side by side.
Fig. 2.9a shows the nature of the supply current for linear load current of 1.7 kA, 0.5 lagging pf before and after the auxiliary converter is turned on. Fig. 2.9b shows the converter, source and load reactive power. As expected the converter reactive current builds up and takes over the source to cater the load reactive power demand.
When the main converter current reaches steady state, the auxiliary converter is turned on. Fig. 2.9c shows the main as well auxiliary converter current. As seen in Fig. 2.9a, the source current turns out to be more of sinusoidal after the auxiliary converter is turned on, which can be considered as a rough evidence (before going in to the detail) of the harmonic elimination role of the auxiliary converter.
Fig. 2.9e shows the load current.
Fig. 2.10 shows the harmonic spectrum before the auxiliary converter is made on. And Fig. 2.11 shows the harmonic spectrum after the auxiliary converter is turned on.
From Figs 2.9 and 2.10 it is found that with only the main converter working, the supply current THD is 8.2 %with the single pulse based case and 7 % with the multi pulse based. When the auxiliary is turned on to eliminate the main converter harmonics and to restrict

the supply current within the specified hysteresis band, in both cases the supply current THD reduces to 4.8 % and 4.78 % respectively.



1) Single pulse PWM for main converter



2) Multi-pulse based SPWM for main converter

Fig. 2.9a. Source voltage and current

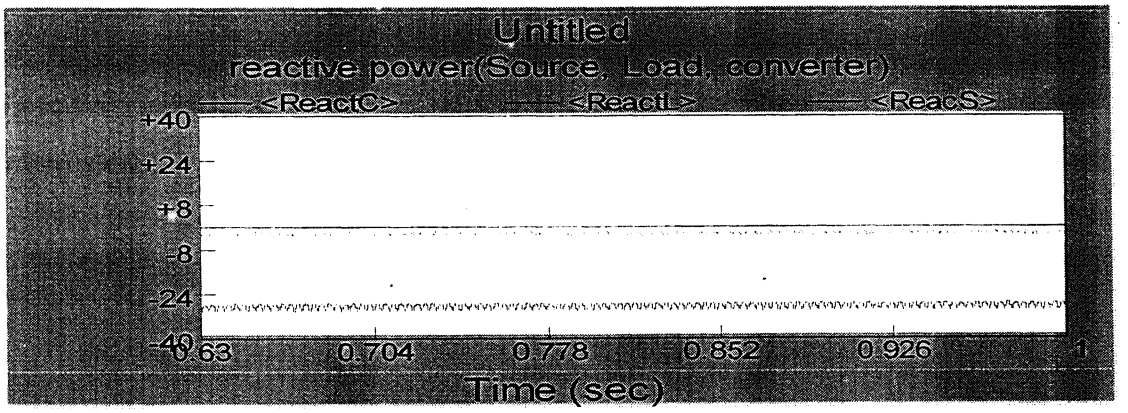
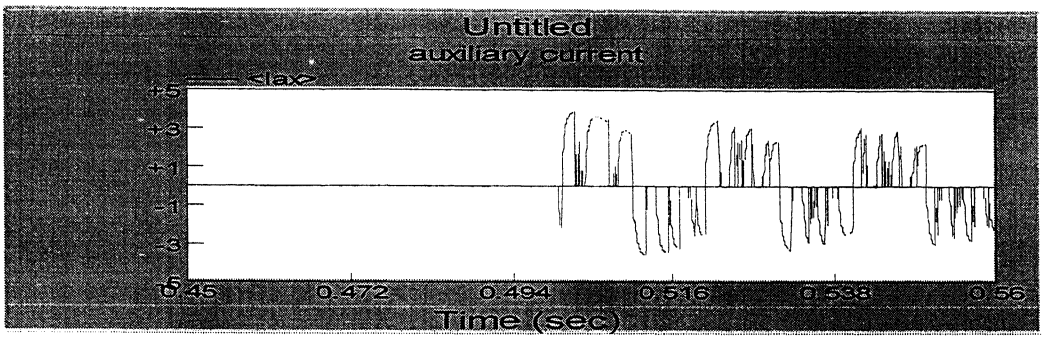
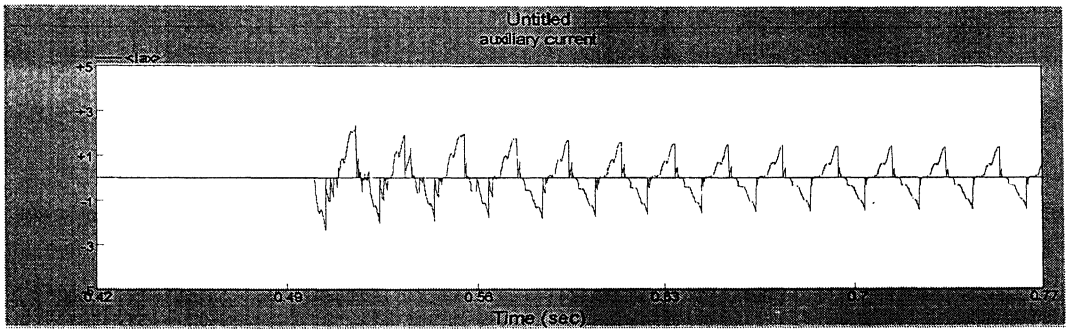


Fig. 2.9b Main converter, source and source reactive



1) Single pulse



2) Multi-pulse

Fig. 2.9c Auxiliary converter current

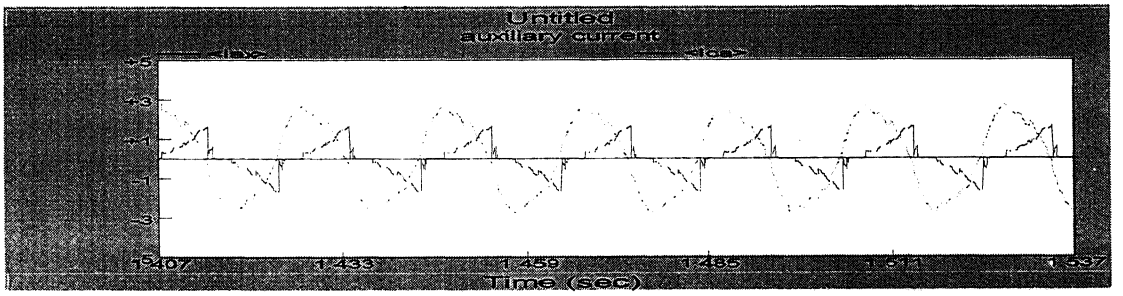


Fig. 2.9d. Main and auxiliary converter currents

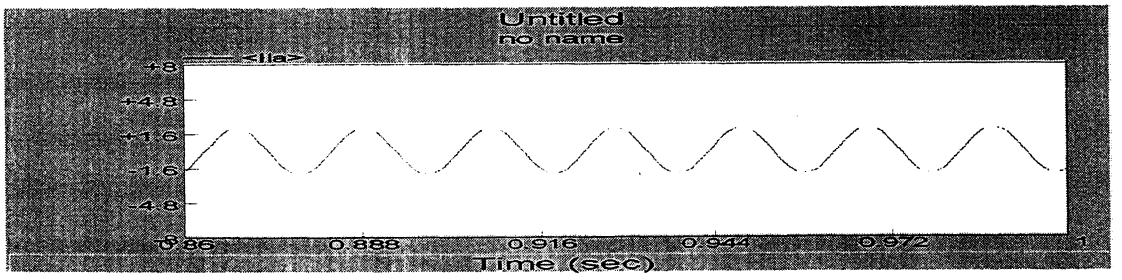


Fig. 2.9e Load current

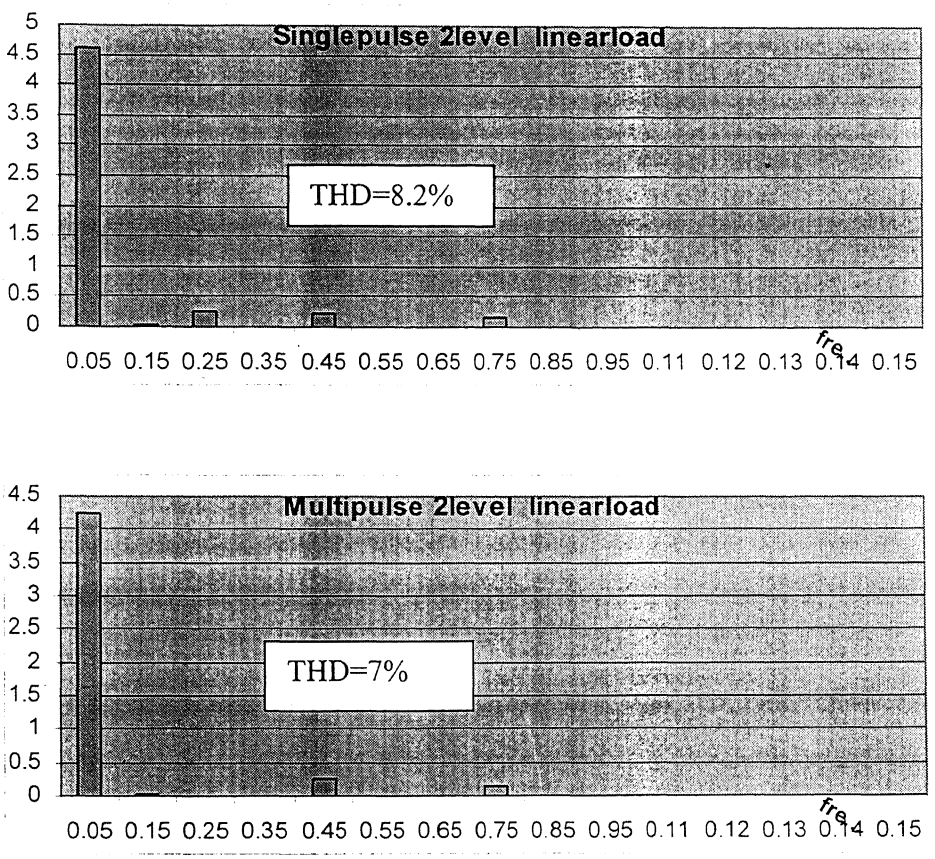
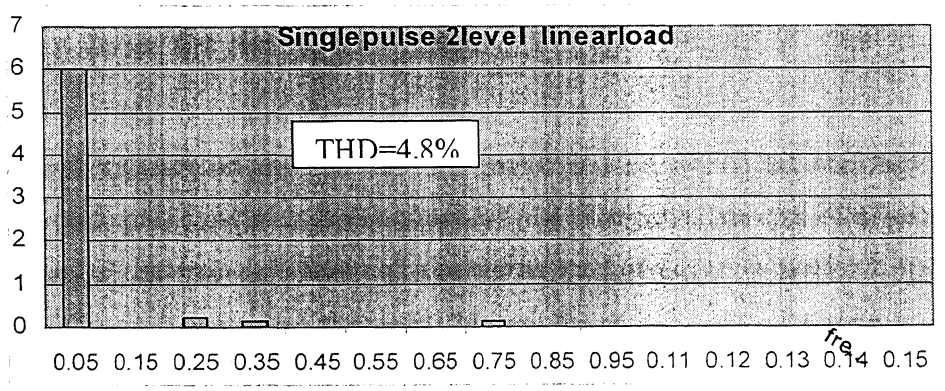


Fig. 2.10. Harmonic spectra of the source current before the auxiliary is turned on



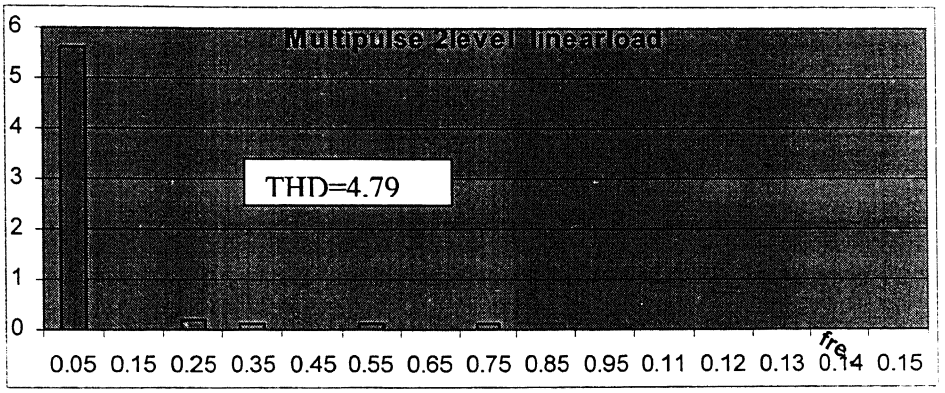


Fig. 2.11 Harmonic spectra of the source current after the auxiliary is turned on

2.5.2 Performance Comparison

In both single pulse and multi pulse based SPWM, the harmonic level before the auxiliary converter is turned on, is a little higher than the IEEE-519 acceptable limits. Despite the switching frequency, which is 6 times higher than the single pulse based, which is manageable with GTOs without severe efficiency deterioration, the multi-pulse based is preferable for the obvious reason of the some what improved converter current output waveform.

2.5.3 Performance of Single and Multi-Pulse SPWM-Based Six-Step Converter for Non-Linear Load.

As already mentioned, an uncontrolled three phase rectifier is used as a non-linear load. Both the single pulse and multi-pulse based SPWM techniques are applied to generate the firing pulses of the main converter and a performance comparison is made.

Fig. 2.12a shows the nature of the supply current for non-linear load current of 1.74 kA, 35.5 MVA, 0.5 lagging pf before and after the auxiliary converter is turned on.

Fig. 2.12b shows the converter, source and load reactive power. As expected the converter reactive current builds up and takes over the source to cater the load reactive power demand.

When the main converter current reaches steady state, the auxiliary converter is turned on. Fig. 2.12c shows the load current.

As seen in Fig. 2.12a, the source current turns out to be more of sinusoidal after the auxiliary converter is turned on, which can be considered as a rough evidence (before going in to the detail) of the harmonic elimination role of the auxiliary converter.

Fig. 2.13a shows the harmonic spectrum before the auxiliary converter is made on. Fig. 2.13b shows the harmonic spectrum after the auxiliary is turned on.

From Figs. 2.13a and b it is found that with only the main converter working, the supply current THD is 19.11% with the single pulse based case, and 16.7 % with the multi pulse based case. When the auxiliary is turned on to eliminate the main converter harmonics and to restrict the supply current within the specified hysteresis band, in both cases the supply current THD reduces to 4.85 % and 4.86 % respectively.

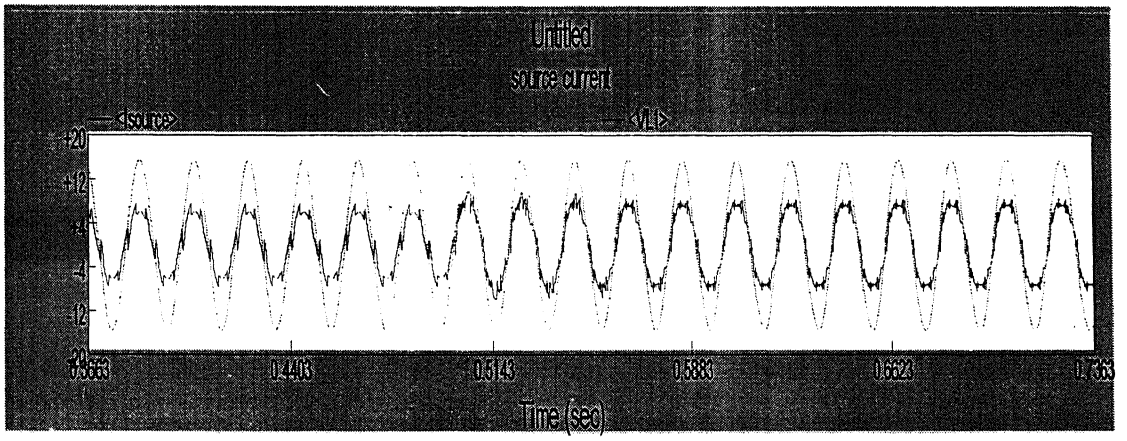


Fig. 2.12 a Source voltage and current

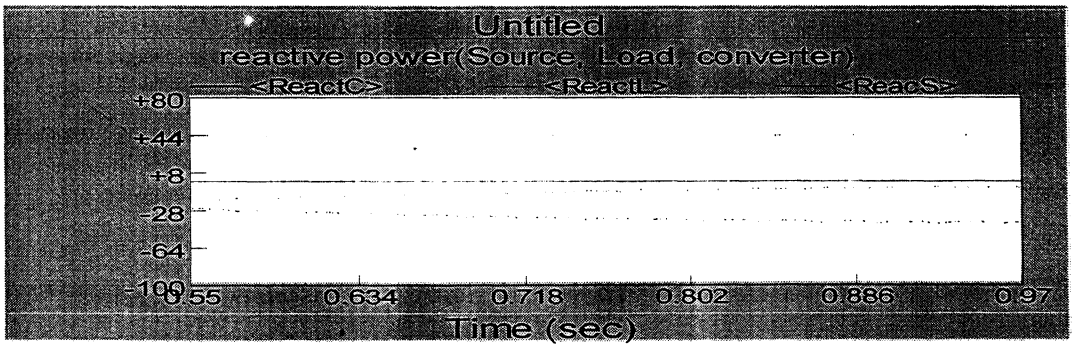


Fig. 2.12b Converter, source and load reactive power

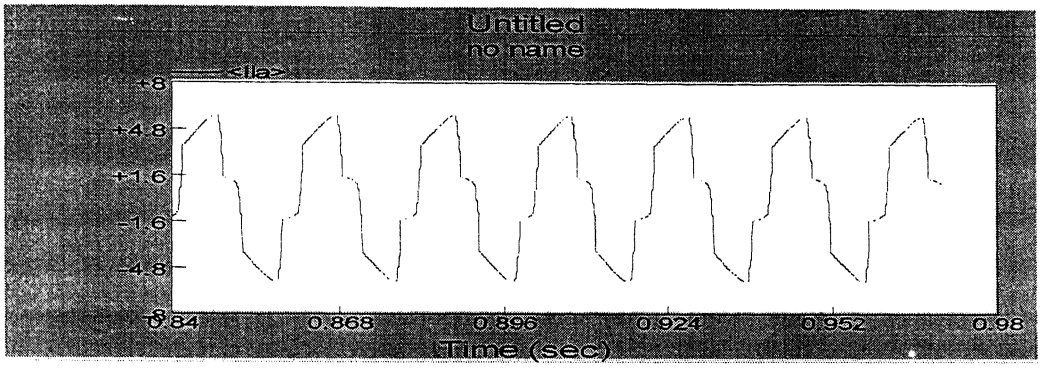


Fig. 2.12c Load current

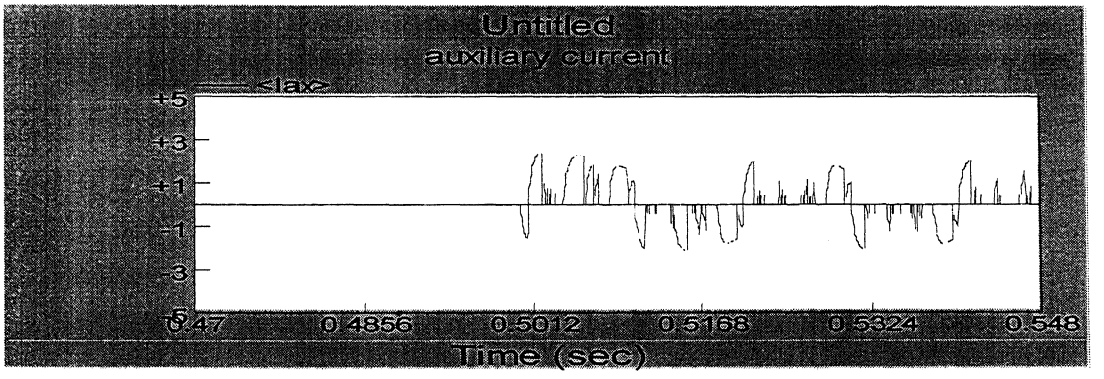
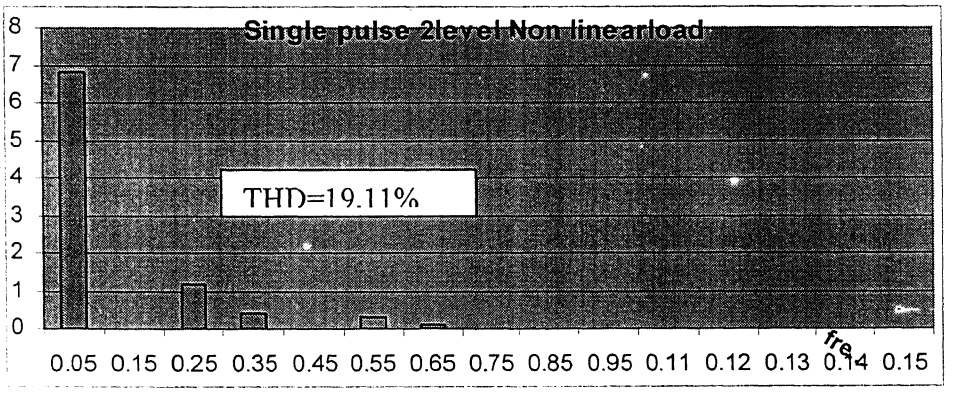


Fig. 2.12d Auxiliary current



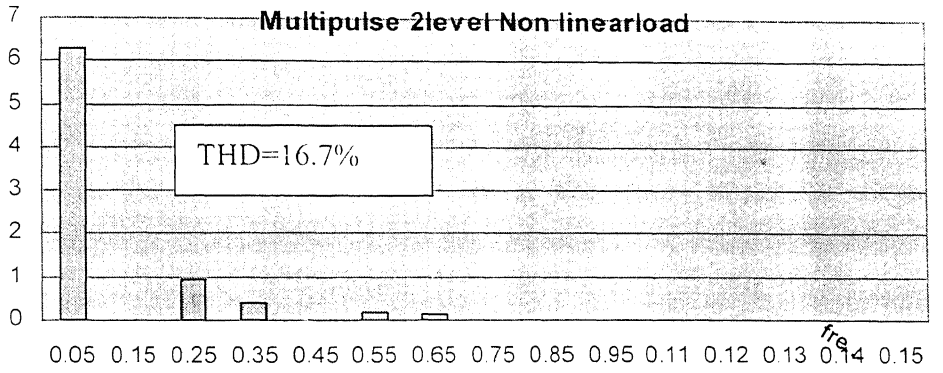


Fig. 2.13a Harmonic spectra, before the auxiliary converter is made on.

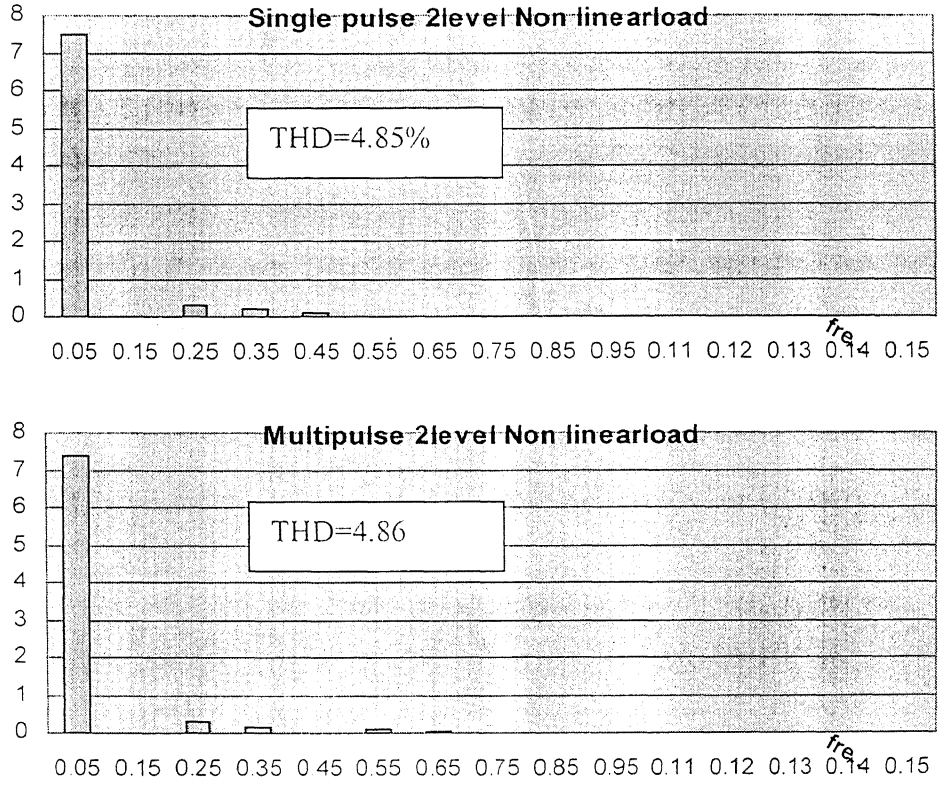


Fig. 2.13b Harmonic spectra, after the auxiliary is turned on.

2.5.4 Performance Comparison

The combined non-linearity effect imposed by both the converter and the non-linear load severely ruins the source current wave shape. The above Figures of the harmonic spectrum are given as evidence to show the distortion level. Even though both cases of single and multi-pulse based SPWM have given a distortion level unacceptable by the IEEE-519, in relative terms, the harmonic content introduced is lower in the multi-pulse based type.

2.6 Conclusion

This chapter has presented the design and simulation aspect of a high power two-level active power filter. A parallel converter topology has been considered. The main converter is operated separately in single pulse and multi-pulse PWM and the performances are compared. The simulation result includes both linear and nonlinear load. The APF is found to be effective in compensating the load harmonic and reactive currents.

CHAPTER 3

Design and Simulation of Three-Level Converter Based Active power Filter (APF)

3.1 Power Circuit Configuration

Here also three phase, three wire, star connected utility is considered. The combined active power filter is connected in parallel to the load as in the six-step.

The main converter used here is a three level (twelve-step) voltage source inverter (VSI), called Neutral Point Clamped Converter, Fig. 3.1 with high power low frequency devices, (GTO).

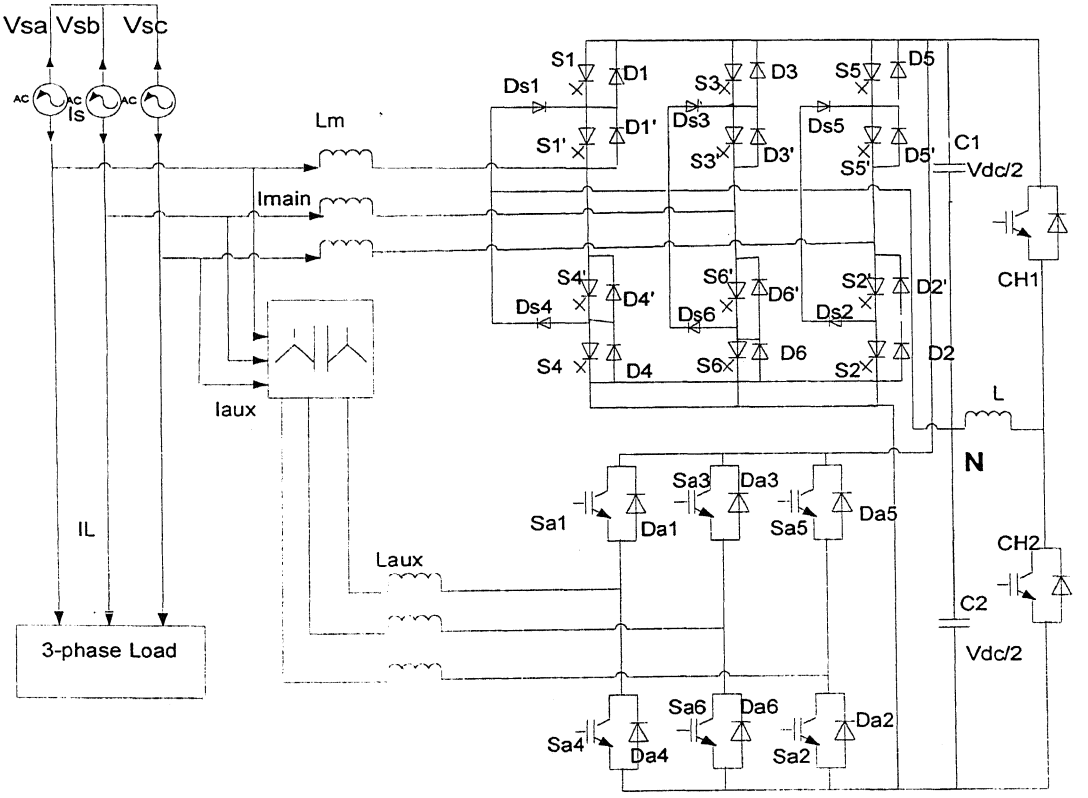


Fig. 3.1 Power circuit configuration of the three-level NPC-APF

The generation of firing pulse trains for the switching devices is made use by both single pulse and multi pulse SPWM techniques and a comparative study is made. In case of the single pulse the switching frequency of the main converter devices is kept to the system frequency so that switching loss is minimized and the full utilization of the current carrying capability of switching devices is realized. In the multi-pulse SPWM case, a switching frequency of 600 Hz (three pulses per quarter cycle) is used. The heating loss with this switching frequency is seemingly affordable as GTO switches are used. Thus, in both cases, the main converter can carry the high reactive power demand of the load.

The auxiliary converter consists of low power high frequency devices (IGBT in this case) controlled by current controlled modulation technique. It eliminates the main converter current harmonics and the load current harmonics from flowing to the utility current by high switching frequency operation.

The two converters share the same dc-link capacitor leading to a compact structure. To avoid circulating currents between the two converters, the auxiliary converter is connected in parallel to the load as well as the main converter with an isolation transformer. This prevents the circulating reactive current between the two converters even though they share the common dc link capacitor.

The effects of both linear and non-linear loads in both the single as well multi-pulse based SPWM have been studied. The non-linear load used here is a simple uncontrolled full bridge rectifier.

3.2 Operating Principle of the NPC VSI

The most popular structure proposed as transformer less voltage source inverter is the neutral point clamped (NPC) converter proposed by Nabae et al [7].

It has the advantages that the blocking voltage of each switching device is one-half of the dc link voltage and the output voltage harmonics content is far less than those of two level converters at the same switching frequency. It has an outweighed advantage in control circuit simplicity and component count than other high level as well three level transformer based converters. In general, the multilevel VSIs unique structure allows

them to reach high voltages with low harmonics with out the use of transformers or series connected synchronized switching devices, a benefit that many contributors have been trying to appropriate for high voltage, high power applications.

The general structure of the multi level converter, which has a multiple of the usual six switches found in a three phase inverter, is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The main motivation for such converters is that current is shared among these multiple switches, allowing a higher converter power rating than the individual switch VA rating would otherwise allow with low harmonics. As the number of levels increase, the synthesized output wave form, a stair case levels like wave, approaches a desired wave form with decreasing harmonic distortion, approaching zero as the number of levels increases.

The structure of the multi-level inverter starts from three level. As aforementioned, the topology is a three-level NPC converter. It consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three level converter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes.

In general for an M-level converter we use:

(M-1)*2* 3 GTO; (M-1)*2*3 diodes in anti-parallel;

(M-1)*(M-2)*3 clamping diodes; and

(M-1) capacitors.

The static VAR compensator implemented here which uses a three level NPC converter of the VSI type shown in Fig. 3.1, therefore, consists of a bridge inverter made of 12 power GTOs with 12 anti-parallel diodes, which is connected to the three phase supply through a tie reactor. Two capacitors are connected to the dc side of the converter and six clamping diodes are used.

The output voltage wave form obtained from this converter is a quasi-square-wave output as shown in Fig. 3.2 a.

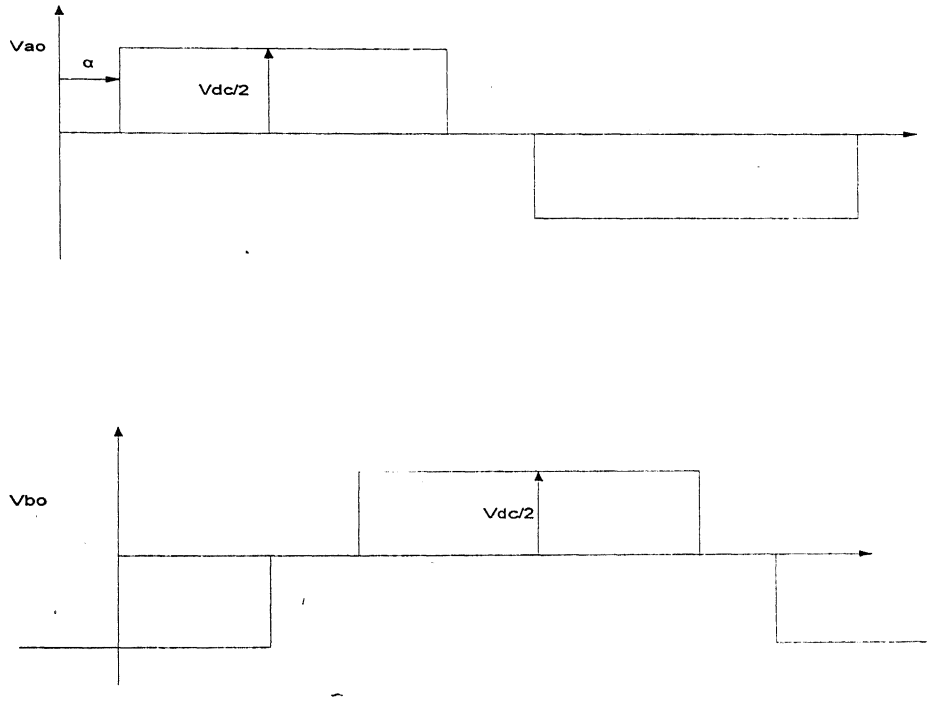


Fig. 3.2a Typical quasi-square phase output voltage of the NPC_VSI

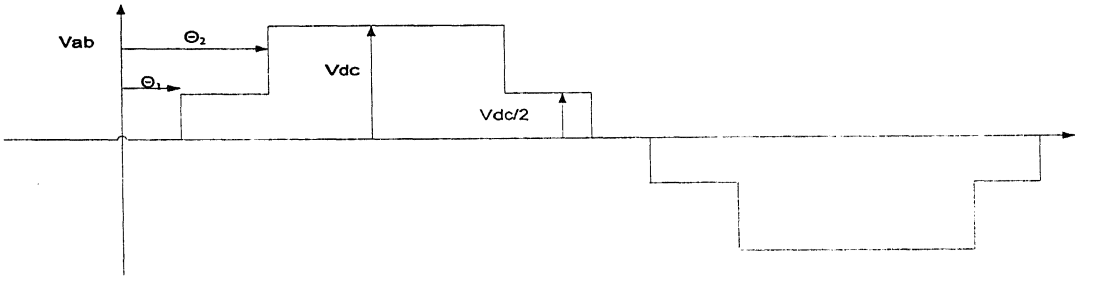


Fig. 3.2b Typical quasi-square L-L output voltage of the NPC_VSI

The over all switching states of the GTO used in the NPC- VSI to obtain the voltages 0, Vd/2 and –Vd/2 is summarized for a single leg referring to Fig 3.1 and 3.2a as in table 3:1 below.

Table 3.1 Switching states for one leg of the NPC-APF

SWITCHES	S1	S1'	S4'	S4	Output voltage
STATES	ON	ON	OFF	OFF	Vd/2
	OFF	ON	ON	OFF	0
	OFF	OFF	ON	ON	-Vd/2

The switches (S1, S4), (S3, S6); (S5, S2) are the main switches; they are switched directly by control pulses. (S'1, S'4), (S'3, S'6); (S'5, S'2) are the auxiliary switches and allow connection of the output of each phase to neutral point (0). Diodes Ds_1-Ds_6 intervene in this operation.

When M is very high, the distortion level is so low that the use of filter is unnecessary. Constraints on switches are low because the switching frequency can be made lower to the line frequency, which is considered in this thesis as single pulse based. As a serious draw back, the excessive number of diodes with an increase in level and the control difficulty of power flow of each converter and control circuit involvement can be mentioned.

In the present scheme, the dc link voltage is not compared with a pre-specified reference. It automatically charges up or down according to the VAR requirement of the load. A chopper circuit is used to keep the two capacitors charged to equal voltage. Whenever one capacitor over charges with respect to the other, a circulating current flows from one capacitor to the other through an inductor of 10 mH, such that the two capacitors are brought back to equal voltage. In the present NPC converter topology the doubling of the number of switches with the same voltage rating makes the dc voltage rating to double, and this increases power handling capability of the converter.

3.3 Harmonic Reduction in the Single Pulse Based Three-Level Inverter

As stated in section 3.2, a trade-ff has to be made between the required number of steps and the design complexity. Harmonics can be reduced as required through PWM voltage control, but as this leads to higher switching frequency of switching devices, it turns out to be inapplicable for high power operation for the obvious reason of switching loss that ruins the efficiency of the converter.

The voltage output waveform for the proposed three level VSI is shown in Fig. 3.2

From the waveform it is evident that it is an odd function, implying that the dc as well the cosine parts of the Fourier transform be zero.

Therefore,

$$V_{con}(\theta) = \frac{1}{\pi}\int_{\alpha}^{180-\alpha}\frac{V_{dc}}{2}\sin n\theta d\theta - \frac{1}{\pi}\int_{180+\alpha}^{360-\alpha}\frac{Vdc}{2}\sin n\theta d\theta$$

$$= \frac{4}{\pi n}\left(\frac{V_{dc}}{2}\cos n\alpha\right) \qquad for\ n = odd\ and\ zero\ for\ n = even \tag{3.1}$$

$$\therefore V_{conv} = \sum_{n}^{\infty}\frac{4}{\pi n}\left(\frac{V_{dc}}{2}\cos n\alpha\right)\sin nwt \qquad for\ n = 1,\ 3,\ 5.....$$

It is obvious that if $\alpha = 18^0$, the fifth harmonic will be zero and if $\alpha = 12.85^0$ the seventh harmonic will be zero, etc.

The line to line output voltage of the proposed single pulse based NPC converter is shown in Fig. 3.2b. The harmonics of this wave form can be expressed as:

$A_n = V_1\cos(n\theta_1) + V_2\cos(n\theta_2)$ [8]

As this wave for is the difference between any two phase voltages, V_1, should be equal to V_2 and θ_1 should be equal to $((\pi/3)-\theta_2)$

$$\therefore A_n = 0.5V_d\left[\cos n\left(\frac{\pi}{3} - \theta_2\right) + \cos(n\theta_2)\right] \tag{3.2}$$

Θ_2 can be selected so as to eliminate any particular harmonic or to reduce the total harmonic distortion. Eliminating only one particular harmonic will not significantly

improve the wave shape; therefore, reducing the total harmonic distortion (THD) is desirable.

Total harmonic distortion can be expressed as

$$THD\% = 100\sqrt{\frac{V_t^2}{V_f^2} - 1} \tag{3.3}$$

Where V_t =rms value of the stepped wave

V_f =rms value of the fundamental for the wave form shown in Fig. 3.2b

$$V_f = \frac{2\sqrt{2}}{\pi}[0.5V\cos\theta_1 + 0.5V\cos\theta_2]$$

$$= \frac{\sqrt{2}}{\pi}V(\cos\theta_1 + \cos\theta_2) \tag{3.4}$$

And

$$V_t = \frac{2}{\pi}\int_{\theta 1}^{\theta 2}(0.5V)^2 d\theta + \frac{2}{\pi}\int_{\theta 2}^{\frac{\pi}{2}}V^2 d\theta \tag{3.5}$$

$$\frac{2V^2}{\pi}\left[\frac{\pi}{2} - 0.75\theta_2 - .25\theta_1\right]$$

$$\therefore \frac{V_t^2}{V_f^2} = \frac{\pi\left[\frac{\pi}{2} - 0.75\theta_2 - .25\theta_1\right]}{(\cos\theta_1 + \cos\theta_2)^2}$$

As $\theta_1 = \pi/3 - \theta_2$ and $\pi/6 \leq \theta_2 \leq \pi/3$

Substituting θ_1 and θ_2 in 3.4 and 3.5

$$V_f = \frac{\sqrt{2}V}{\pi}\left[\cos\left(\frac{\pi}{3} - \theta_2\right) + \cos\theta_2\right]$$

$$V_t^2 = \frac{2V^2}{\pi}\left[\frac{\pi}{2} - 0.75\theta_2 - .25\left(\frac{\pi}{3} - \theta_2\right)\right]$$

$$= \frac{2V^2}{\pi}\left[\frac{5\pi}{12} - 0.5\theta_2\right]$$

Therefore

$$\frac{V_t^2}{V_f^2} = \frac{\frac{2V^2}{\pi}\left[\frac{5\pi}{12} - 0.5\theta_2\right]}{\frac{2V^2}{\pi^2}\left[\cos\left(\frac{\pi}{3} - \theta_2 + \cos\theta_2\right)\right]^2} \qquad (3.6)$$

$$= \frac{\pi\left[\frac{5\pi}{12} - 0.5\theta_2\right]}{\left[\cos\left(\frac{\pi}{3} - \theta_2\right) + \cos\theta_2\right]^2}$$

To minimize the total harmonic distortion the term $\frac{V_t^2}{V_f^2}$ should be minimum. This is obtained by equating the differential of this term with respect to θ to zero.

Let $y = \frac{V_t^2}{V_f^2}$

$$\therefore \frac{dy}{d\theta} = 0$$

$$= \left[\cos\left(\frac{\pi}{3} - \theta_2\right) + \cos\theta_2\right]^2 [-0.5] + 2\left[\frac{5\pi}{12} - 0.5\theta_2\right]\left[\cos\left(\frac{\pi}{3} - \theta_2\right) + \cos\theta_2\right]\left[\sin\theta_2 - \left(\frac{\pi}{3} - \theta_2\right)\right]$$

$$\Rightarrow \frac{dy}{d\theta} = \left(\frac{5\pi}{3} - 2\theta_2\right) - \frac{\cos\left(\frac{\pi}{3} - \theta_2\right) + \cos\theta_2}{\sin\theta_2 - \sin\left(\frac{\pi}{3} - \theta_2\right)} = 0$$

As shown in [9] too, numerical solution gives $\theta_2 = 45.303^0$ and, therefore $\theta_1 = 15^0$. The harmonic amplitudes for two waveforms, namely, the conventional and the one with a THD improvement method, are given in a table in [8]. The significant reduction in the THD from 31.8% in the conventional waveform to 16.86 % in the proposed waveform is remarkable. At the same time, the dominant 5^{th} and 7^{th} harmonics are also reduced from 20% to 5.35% and 14.5% to 3.82 % respectively.

3.4 Harmonic Analysis of the Three-Level PWM Waveform

The Fourier Expression for a wave form with odd quarter wave symmetry is given by:

$$e(wt) = \sum_{1}^{\infty} A_n \sin nwt \qquad (3.7)$$

Where n is an odd number and

$$A_n = \frac{4}{\pi} \int_{o}^{\frac{\pi}{2}} f(wt)\sin(nwt)d(wt) \qquad (3.8)$$

For analysis purpose the three level single pulse waveform in Fig 3.2 is considered. Accepting some constraints, symmetrical or uniform pwm technique can be applied to such a waveform [8].

The basic constraint to be followed in three-level inverter is to have odd quarter wave symmetry for a line-to-line voltage waveform. To have this symmetry the 150^0 conduction period is divided.in to five equal segments. Ideally each segment can have any number of equal width pulses. In this thesis, three pulses per quarter cycle is considered.

If m is any integer 1, 2, 3...m, then to have the quarter wave symmetry in an L_L wave form, the chopping frequency of the fixed amplitude triangle carrier should be 12mf, where f is the output wave form. With this condition satisfied, it follows that:

1. the numbers of pulses per half cycle of the phase voltage wav e form will be 6m
2. the number of pulses in the half cycle of a line voltage will be 5m;
3. the spacing between the center of each pulse will be π/6m rad;
4. there will be 2m number of pulses with the amplitude equal to 0.5E
5. the number of pulses with the amplitude equal to E will be 3m;
5. the first pulse will be spaced at (π/12) + (π/12 m) rad from the reference axis.
6. if δ is the variable pulse width of a pulse, the theoretical maximum pulse width will be $\Delta = \pi$/6m rad.

The analysis of a generalized line-to-line voltage with 5m number of pulses per half cycle will be divided in two parts, a) when m is odd and b) when m is even.

Recalling the constraints an the resulting output voltage

$$A_n = \frac{4}{\pi}\int_{\frac{\pi}{12}(1+\frac{1}{m})-\frac{\delta}{2}}^{\frac{\pi}{12}(1+\frac{1}{m}+\frac{\delta}{2}} 0.5E\sin(nwt)d(wt) + \frac{4}{\pi}\int_{\frac{\pi}{12}(1+\frac{1}{m})+\frac{\pi}{6m}-\frac{\delta}{2}}^{\frac{\pi}{12}(1+\frac{1}{m})+\frac{\pi}{6m}+\frac{\delta}{2}} 0.5E\sin(nwt)d(wt) + \ldots\ldots\ldots$$

$$+\frac{4}{\pi}\int_{\frac{\pi}{12}(1+\frac{1}{m})+(p-1)\frac{\pi}{6m}-\frac{\delta}{2}}^{\frac{\pi}{12}(1+\frac{1}{m})+(p-1)\frac{\pi}{6m}+\frac{\delta}{2}} 0.5E\sin(nwt)d(wt) + \frac{4}{\pi}\int_{\frac{\pi}{4}+\frac{\pi}{12m}-\frac{\delta}{2}}^{\frac{\pi}{4}+\frac{\pi}{12m}+\frac{\delta}{2}} 0.E\sin(nwt)d(wt) + \ldots\ldots\ldots$$

$$+\frac{4}{\pi}\int_{\frac{\pi}{4}+\frac{\pi}{12m}+(p-1)\frac{\pi}{6m}-\frac{\delta}{2}}^{\frac{\pi}{4}+\frac{\pi}{12m}+(p-1)\frac{\pi}{6m}+\frac{\delta}{2}} E\sin(nwt)d(wt) + \frac{4}{\pi}\int_{\frac{\pi}{2}-\frac{\delta}{2}}^{\frac{\pi}{2}} E\sin(nwt)d(wt)$$

$$\therefore A_n = \frac{2E}{n\pi}\left[\sum_{p=1}^{\infty}\left[\cos n\left[\left(\frac{2p-1}{m}+1\right)\frac{\pi}{12}-\frac{\delta}{2}\right]-\cos n\left[\left(\frac{2p-1}{m}+1\right)\frac{\pi}{12}+\frac{\delta}{2}\right]\right]+\right.$$

$$+\frac{4E}{n\pi}\sum_{p=1}^{1.5m-0.5}\left[\cos n\left[\left(\frac{2p-1}{m}+3\right)+\frac{\pi}{12}-\frac{\delta}{2}\right]-\cos n\left[\left(\frac{2p-1}{m}+3\right)\frac{\pi}{2}+\frac{\delta}{2}\right]\right]$$

$$\left.+\frac{4E}{n\pi}\cos n\left(\frac{\pi}{2}-\frac{\delta}{2}\right)\right]$$

$$\therefore A_n == \frac{4E}{n\pi}\left[\sum_{p=1}^{m}\left(\sin\left(\sin\frac{n\pi}{12}\left(\frac{2p-1}{m}+1\right)\right)\sin(\frac{n\delta}{2})\right)\right] \qquad (3.9)$$

$$+2\sum_{p=1}^{1.5m-0.5}\left(\sin\left(\frac{n\pi}{12}\left(\frac{2p-1}{m}+3\right)\right)\sin\frac{n\delta}{2}\right)+\left(\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\delta}{2}\right)\right)$$

Similarly when n is even

$$An=\frac{4E}{n\pi}\left[\sum_{p=1}^{m}\left(\sin\left(\frac{n\pi}{2}\left(\frac{2p-1}{m}+1\right)\right)\sin\left(\frac{n\delta}{2}\right)\right)\right]+\frac{4E}{n\pi}\left[\sum_{p=1}^{1.5m}\left(2\sin\frac{n\pi}{12}\left(3+\frac{2p-1}{m}\right)\sin\left(\frac{n\delta}{2}\right)\right)\right]$$

For the specific case of m=1, which is used in this thesis equation 3.9 becomes:

$$An=\frac{4E}{n\pi}\left[\sin\left(\frac{n\pi}{6}\sin\frac{n\delta}{2}+2\sin\frac{n\pi}{3}\sin\frac{n\delta}{2}+\sin\frac{n\pi}{2}\sin\frac{n\delta}{2}\right)\right] \tag{3.10}$$

If k is the relative pulse width $\frac{\delta}{\Delta}$ where $\Delta=\frac{\pi}{6m}$

$$An=\frac{4E}{n\pi}\sin\frac{nk\pi}{12}\left[\sin\frac{n\pi}{6}+2\sin\frac{n\pi}{3}+\sin\frac{n\pi}{2}\right] \tag{3.11}$$

3.5 Control Strategy

A VSI, in general, comprises a large number of gate controlled semi conductor power switches. The gating commands for these devices are generated by the internal converter control in response to the demand for reactive and/or real power reference signal(s). In this thesis as aforementioned, use is made by SPWM and a different method of harmonic elimination [11-14] is used as we are dealing with a multi level.

In general one of the problems in controlling a VSI with variable amplitude and frequency of the output voltage is to obtain an output waveform as much as possible of sinusoidal shape employing simple control techniques. Indeed current harmonics caused by non-sinusoidal voltage feeding imply power losses, electromagnetic interference, and pulsating torques in ac motor drives. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy.

Under the aspect of harmonic content reduction, multilevel inverters are of the highest importance despite the control complexity and devices involved. They are particularly suitable in high power applications when the semiconductor devices are not able to operate at high switching frequencies. It is also worth to note that, when adopting traditional bipolar inverter topologies very high powers cannot be obtained unless using problematic series/parallel combinations of the solid state switches which further lower

the highest possible switching frequencies.[15,16] The multilevel structures allow to raise the power handled in the conversion process in a very natural way.

A VSI which allows multilevel operation if the number of level $n \geq 3$, having more than two voltage levels to build a sinusoidal shape it is intuitive that we can have reduction of the current harmonics in the load [3]. Nevertheless, the actual improvement of the current spectrum depends on the control technique employed.

Among the different arrangements the carriers are supposed to have, the idea of using several triangular carrier signals, [17, 18] keeping only one modulating sinusoidal signal is considered. For example if an N-level inverter is employed, N-1 carriers will be needed. The carriers will have the same frequency and the same peak-to-peak amplitude and are disposed so that the bands they occupy are contiguous. The modulating signal is a sinusoidal of frequency equal to the expected output fundamental voltage. At every instant each carrier is compared with the modulating signal. Each comparison gives 1(-1) if the modulating sinusoid is greater than (lower than) the triangular carrier in the first and second half of the fundamental period, and zero otherwise. The results are added to give the voltage level, which is required at the output terminal of the converter. Obviously, the actual driving signals for the power devices opened on the particular structure chosen to realize the inverter and thus can be derived from the results of the modulating-carriers comparison by means of a simple logic circuit.

In this case, therefore, as we are dealing with three level, two carriers separated from each other by 180^0 are considered, Fig. 3.3 and each compared with a common sinusoidal signal, and the two resulting carrier-sinusoidal comparison are added to give the expected pulses that will trigger the gates in a way that the converter should give the expected output voltage wave form shown in Fig. 3.4

The control angle δ is here used to modify the modulating signal in such a way that a shift of it with respect to the carrier triangular waveform should take place, which is indirectly an indication of the loss component of the converter.

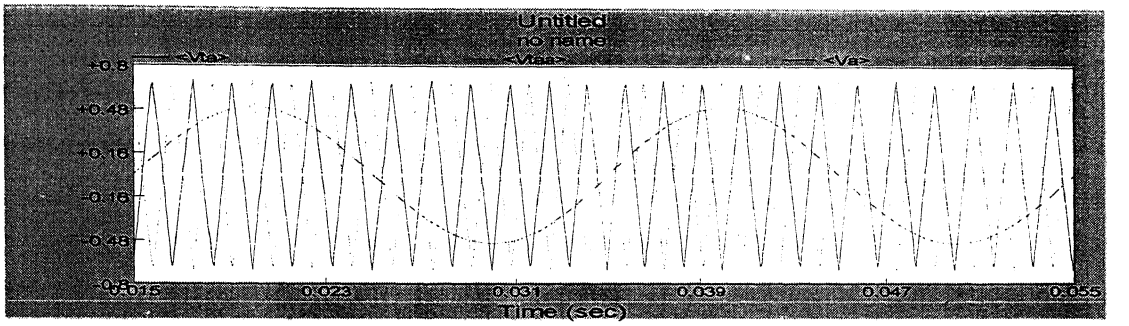


Fig. 3.3 The two carriers separated by 180^0 to be compared with single sinusoidal wave

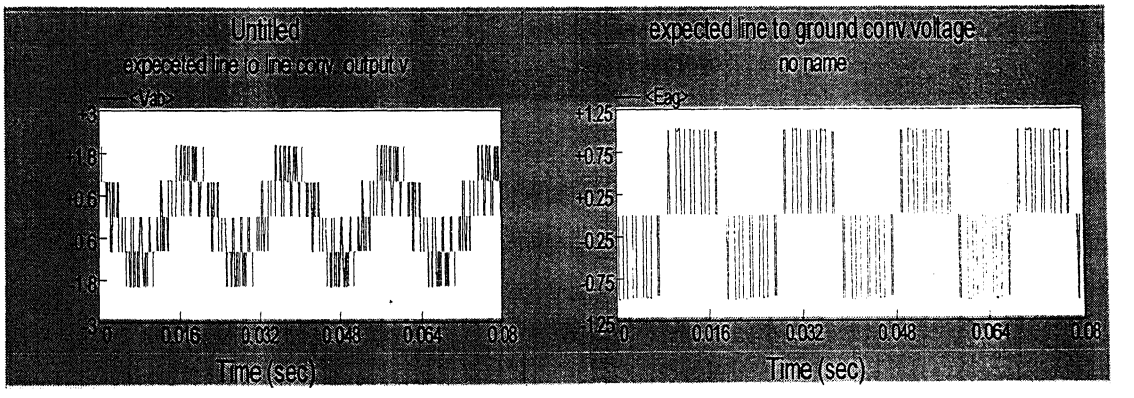


Fig. 3.4 Expected output line and phase voltages

3.6 Estimation of Reference Current and Delta

The complete system control block diagram for the 12-step –APF is given in Fig. 3.5.

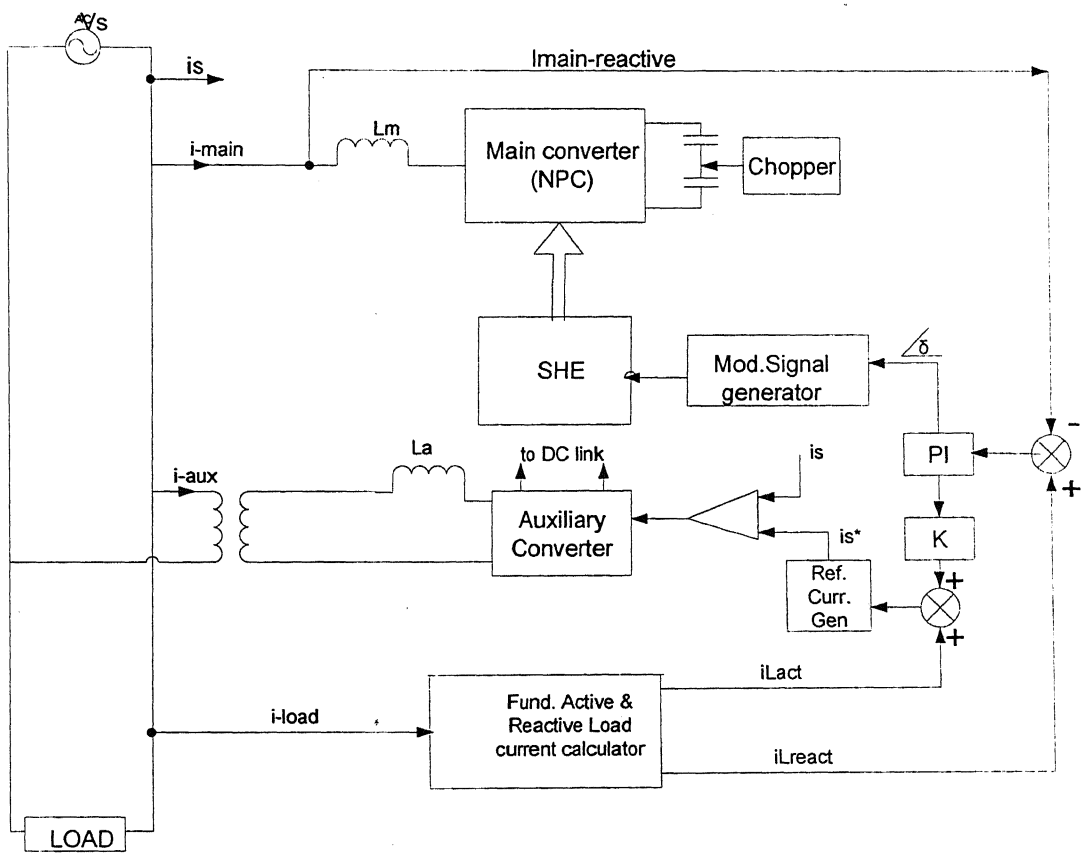


Fig. 3.5 Control block diagram of the proposed compensator scheme of NPC_APF

As the need and ultimate goal of reactive compensation, the utility should supply only the active component of load current and the loss component of the converter at unity power factor. Therefore, the supply current should always be in phase with the respective phase voltage.

The angle δ is determined in such a way that, the actual reactive current that is coming from the compensator is deducted from the load reactive current requirement, which can be referred to as the reactive reference current. The error signal is processed through a PI controller and a limiter to generateδ.

In ideal case, angle δ is supposed to be zero, as the main converter current provides only the load reactive current, which is at quadrature with the supply voltage. However, because of the converter losses, the capacitor voltage tends to fall and requires small amount of active current from the supply to maintain the charge. So the angle δ acts as a measure of converter losses.

To determine the reference magnitude of the source current, a control signal proportional to δ is added with the active component of the load current I_{Lact}. This amplitude multiplied by a sin-template (in phase with the utility phase voltage) gives the reference utility current I_{sref} for the respective phase. These reference currents have to do with the auxiliary converter.

A sinusoidal reference current I_{sref} in phase with the utility voltage is synthesized and the source current Is is forced to follow this reference with a hysteresis band. The source current is sensed and compared with the reference current. The error thus obtained decides the switching instants of the auxiliary compensator devices.

Current in each phase is controlled independently. In order to increase the current of a particular phase, lower devices of the auxiliary compensator associated with that phase, is turned on. While for decreasing the current, upper device associated with that particular phase is turned on.

$$\begin{aligned} I_{ref} &= k \times \delta + I_{Lp} \\ Isref(a) &= I_{ref} \sin \omega t \\ Isref(b) &= I_{ref} \sin(\omega t - 120^{\circ}) \\ Isref(c) &= I_{ref} \sin(\omega t + 120^{\circ}) \end{aligned} \qquad (3.12)$$

Where k is determined judiciously

The following approach is used to determine delta:

$$P = \frac{1}{T} \int vidt \qquad (3.13)$$

$$let\ v_a = v \sin wt$$

And

$$va^{I} = v \sin(wt - \frac{\pi}{2})$$

$$\Rightarrow \frac{1}{T}\int v_a i_a dt = \frac{I_{mp}V_m}{2} \tag{3.14}$$

I_{mp} is the active current component

and $$\frac{1}{T}\int v_a^I i_a dt = \frac{I_{mq}V_m}{2} \tag{3.15}$$

Where I_{mq} is the reactive component of the current

Both the load and the converter reactive current components are taken this way, compared, processed by a PI controller and resulted delta as shown in Fig. 3.5

3.7 Simulation Results

As in the case of the two levels, for ease of comparison, the same procedure followed in the presentation; a load of a given MVA is connected to the system voltage in parallel with the main converter. The main converter is here also seen building up and taking over the reactive demand of the load from the source. As the converter current gets stable, the auxiliary converter is made on. A detailed analysis, as to whether the harmonic level before turning on the auxiliary converter was un acceptable according to IEEE-519 standard or not and whether the auxiliary converter made the harmonics to an acceptable level, is made graphically as well mathematically by using the harmonic spectrums and THD respectively, and results are given in similar fashion as that of the two level case.

The dynamics performance is studied by changing the load current magnitude for some time and then bringing back to the previous value. The effect of increasing the load current is given graphically to consolidate the study.

3.7.1 Performance of Single and Multi-Pulse Based NPC-APF for VAR Compensation of Linear Loads

Steady State response

A three phase star connected 40 MVA linear load is considered in a 7.78 kV rms three phase three wire system. For comparison purposes, results obtained from both cases. (by which firing pulse generation for the main converter is made by use of single pulse and multi-pulse SPWM) are given side by side.

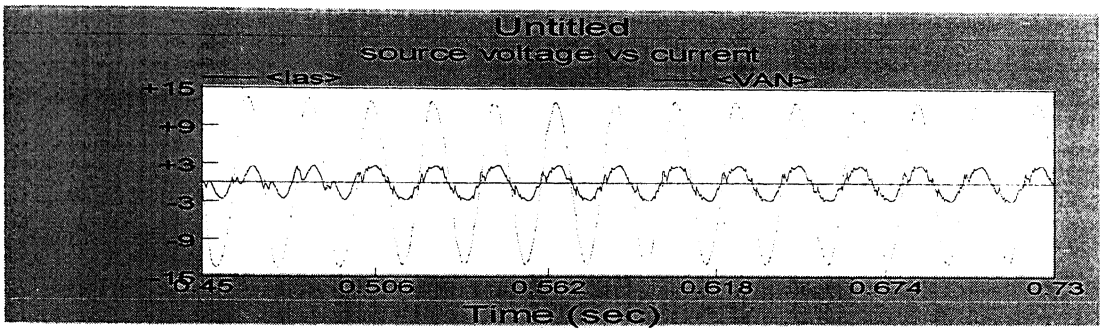
Fig. 3.6a shows the nature of the supply current for linear load current of 2.8 kA, 0.5 lagging pf before and after the auxiliary converter is turned on. Fig. 3.6b shows the converter, source and load reactive power. As expected the converter reactive current builds up and takes over the source to cater the load reactive power demand.

When the main converter current reaches steady state, the auxiliary converter is turned on. Fig. 3.6c shows the main as well auxiliary converter current. As seen in Fig. 3.6a, the source current turns out to be more of sinusoidal after the auxiliary converter is turned on, which can be considered as a rough evidence (before going in to the detail) of the harmonic elimination role of the auxiliary converter.

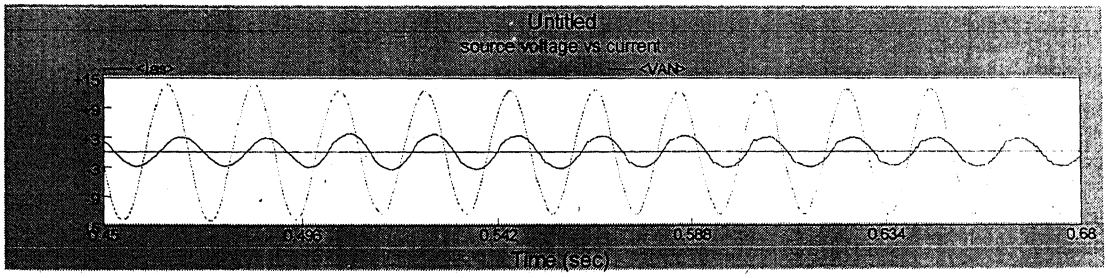
Fig. 3.7 shows the dc–link voltage.

Fig. 3.9a shows the harmonic spectra before the auxiliary converter is made on. And Fig. 3.9b shows the harmonic spectra after the auxiliary is turned on.

From Figs 3.9a and b it is found that with only the main converter working, the supply current THD is 5.19% with the single pulse based case and 4.97 % with the multi-pulse based. When the auxiliary is turned on to eliminate the main converter harmonics and to restrict the supply current within the specified hysteresis band, in both cases the supply current THD reduces to 4.7 % and 3.6 % respectively.



1) Single pulse



2) Multi-pulse

Fig. 3.6a Source Voltage and current

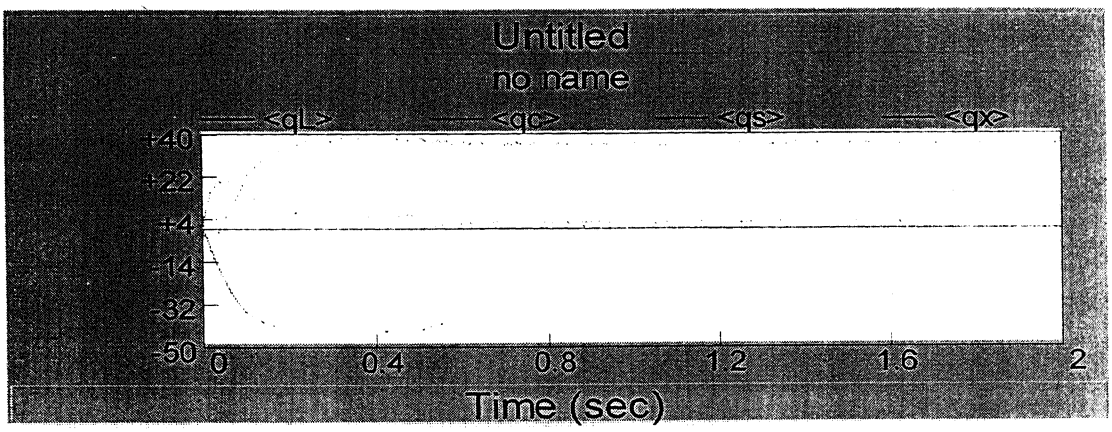


Fig. 3.6b Source, main and auxiliary converter and load reactive current

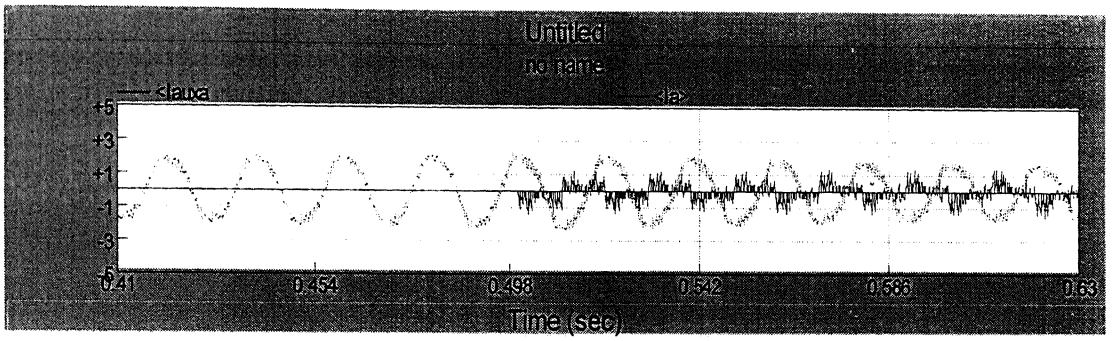


Fig. 3.6c Main and auxiliary converter current

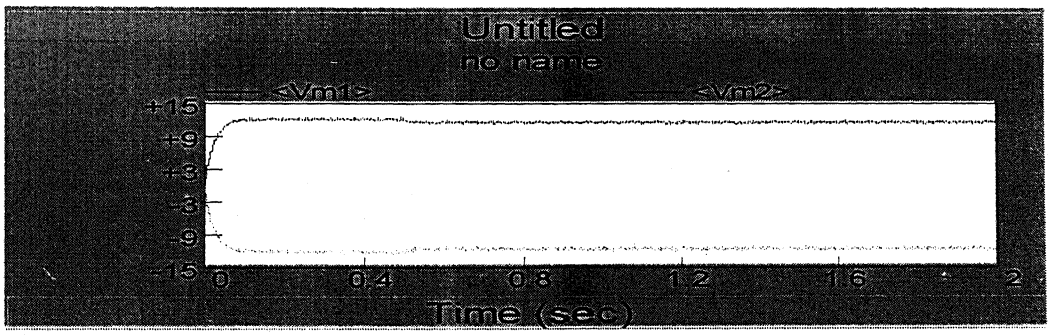
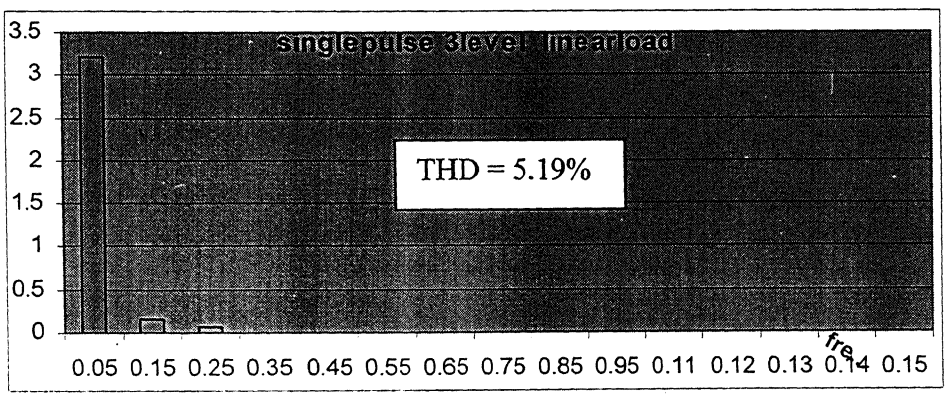


Fig. 3.7 Dc-link voltage



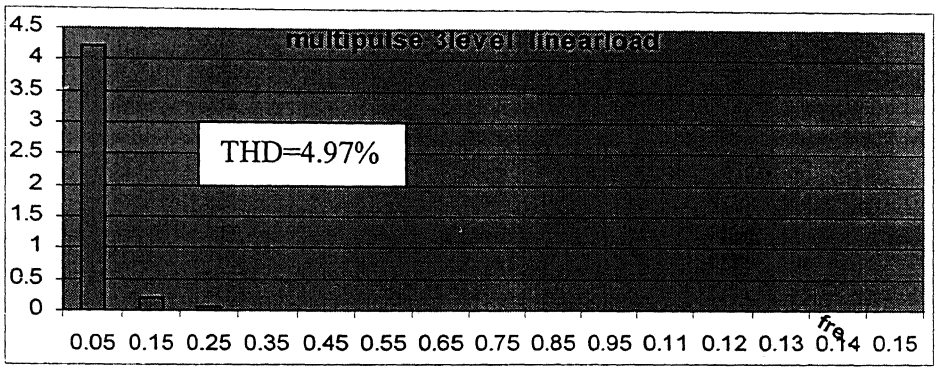
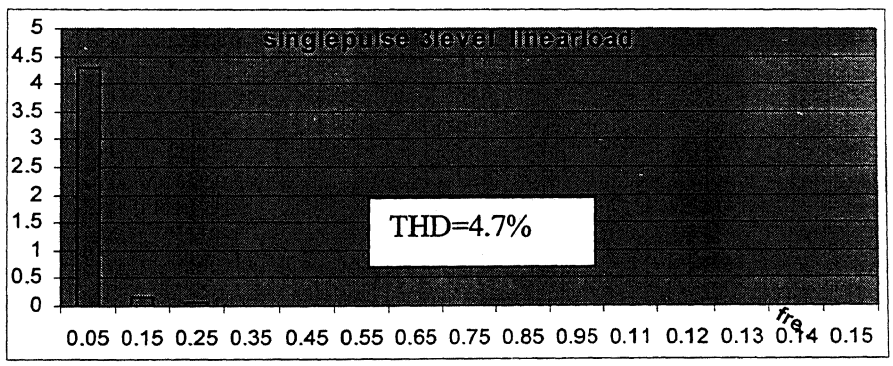


Fig. 3.9a Harmonic spectra before the auxiliary converter is made on



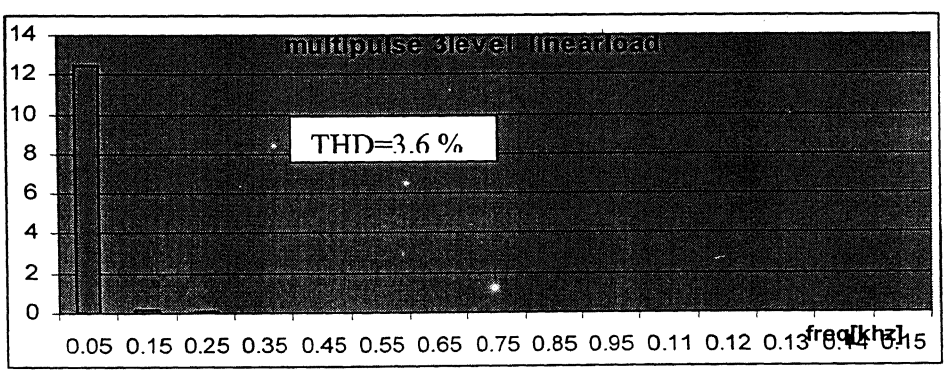


Fig. 3.9b Harmonic spectra after the auxiliary converter is made on

Dynamic Performance

The dynamic performance of this linear load based system is studied by changing the load current from 2.8 kA and to 3.5 kA and then bringing back to the previous value.

As shown in Fig. 3.10 the supply current remains in phase with the supply voltage. As the change encountered in the load current has to be compensated, a change in the magnitude of either of the converters output current is expected.

Fig. 3.11 shows the increment of the auxiliary converter current and its reduction after the build up of the main converter current. It shows the fast response of the direct current controlled auxiliary converter, to take care of the transient change in the reactive demand of the load which will eventually be taken care of by the relatively low response main converter which indirectly controlled by shifting the fundamental voltage of the main converter by angle delta.

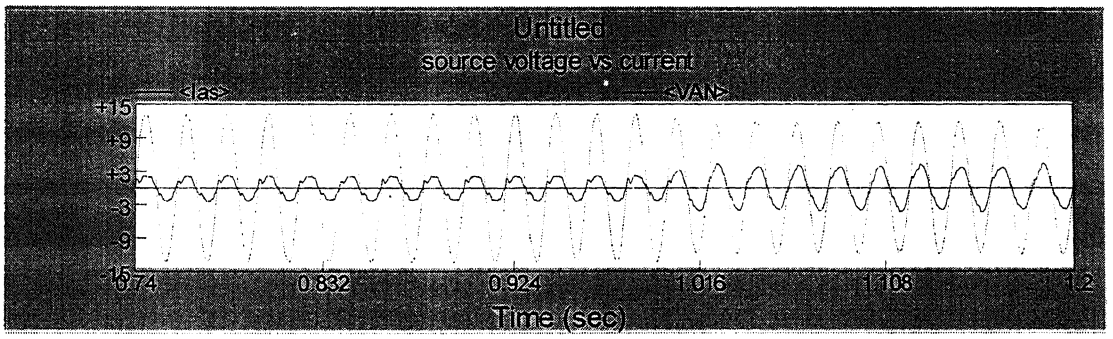


Fig. 3.10 Source voltage and current in phase even after load change

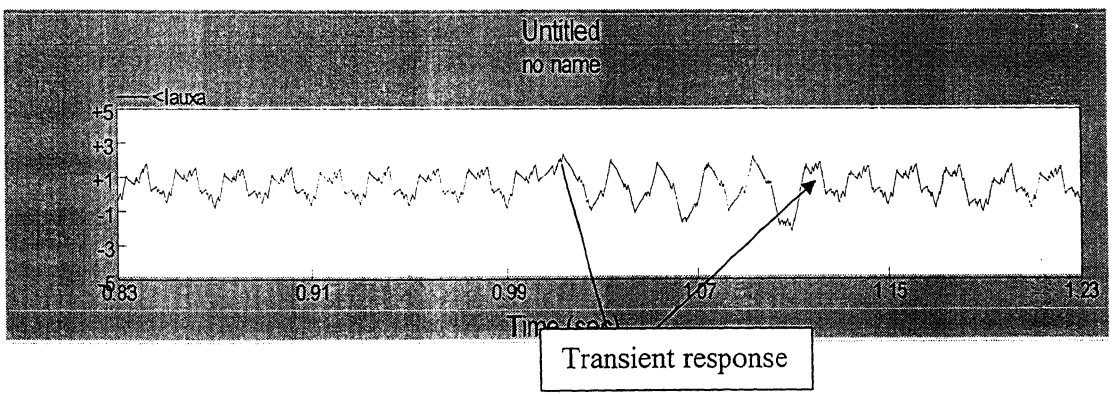


Fig. 3.11 Auxiliary current

3.7.2 Performance Comparison

Despite the relatively higher switching frequency (600 Hz) used in the multi-pulse case, which of course, is believed to be manageable for the GTO with no significant efficiency deterioration, the main converter output current is found to be more sinusoidal compared to its single pulse based counter part. This obviously shows the reduced harmonic intrusion in to the line compared to the single pulse based.

3.7.3 Performance of Single and Multi-Pulse SPWM-Based NPC-APF for Non-linear Load.

As already mentioned, an uncontrolled three-phase rectifier is used as a non-linear load. Both the single pulse and multi pulse based SPWM techniques are applied to generate the firing pulses of the main converter and a performance comparison is made.

Fig. 3.12a shows the nature of the supply current for non-linear load current of 5 kA, before and after the auxiliary converter is turned on. Fig. 3.12b shows the converter, source and load reactive power. As expected the converter reactive current builds up and takes over the source to cater the load reactive power demand.

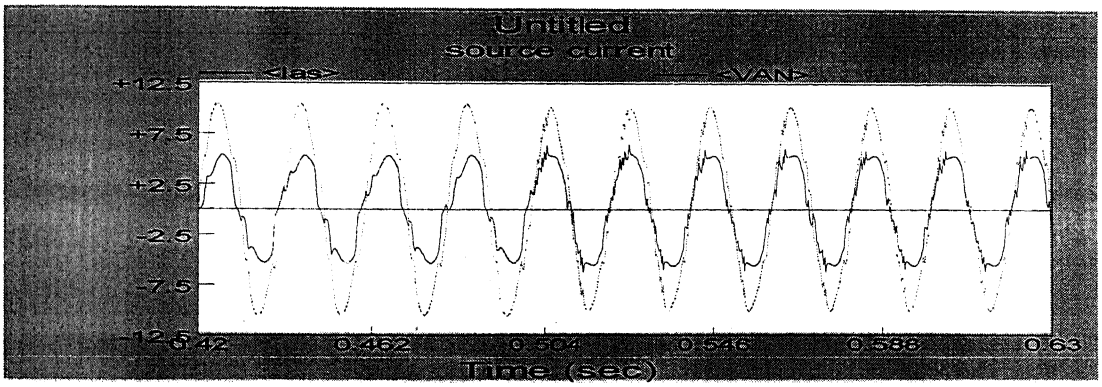
When the main converter current reaches steady state, the auxiliary converter is turned on. Fig. 3.12c shows the load current.

As seen in Fig. 3.12a, the source current turns out to be more of sinusoidal after the auxiliary converter is turned on, which can be considered as a rough evidence (before going in to the detail) of the harmonic elimination role of the auxiliary converter.

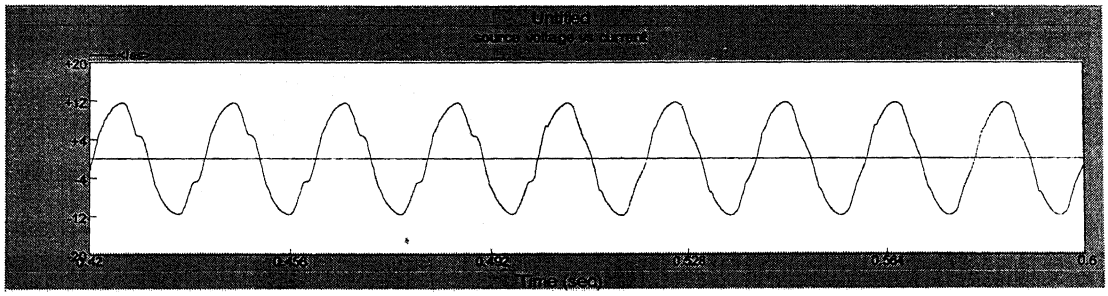
Fig. 3.13a shows the harmonic spectra before the auxiliary converter is made on. And Fig. 3.13b shows the harmonic spectra after the auxiliary is turned on.

From Figs 6.2a and b it is found that, with only the main converter working, the supply current THD is 15.4% with the single pulse based case and 11.4 % with the multi pulse based. When the auxiliary is turned on to eliminate the main converter harmonics and to

restrict the supply current within the specified hysteresis band, in both cases the supply current THD reduces to 4.67 % and 4.11 % respectively.



1) Single pulse based



2) Multi pulse based

Fig. 3.12a Source voltage and current before and after the auxiliary is turned on

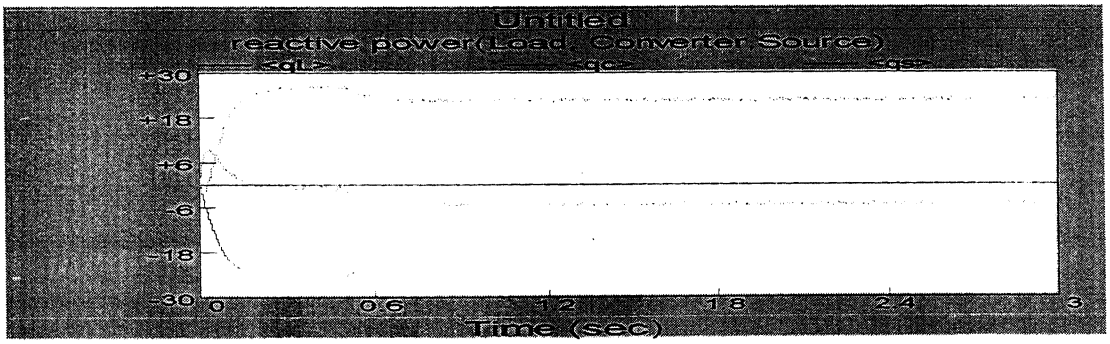
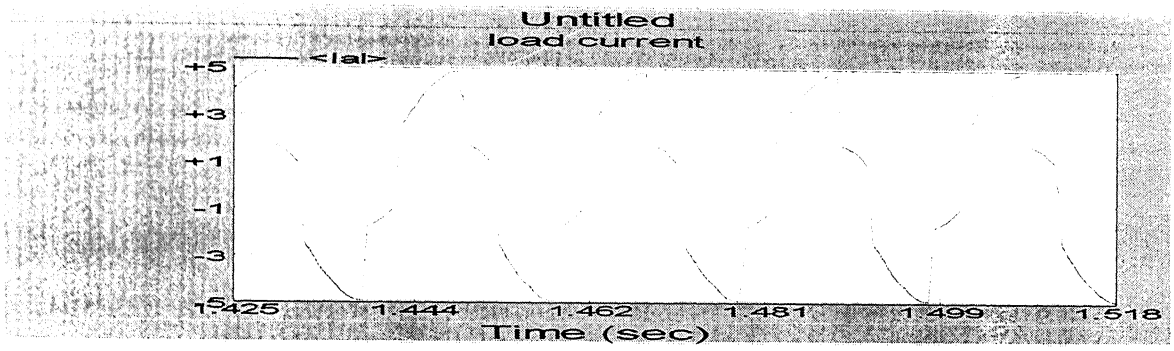
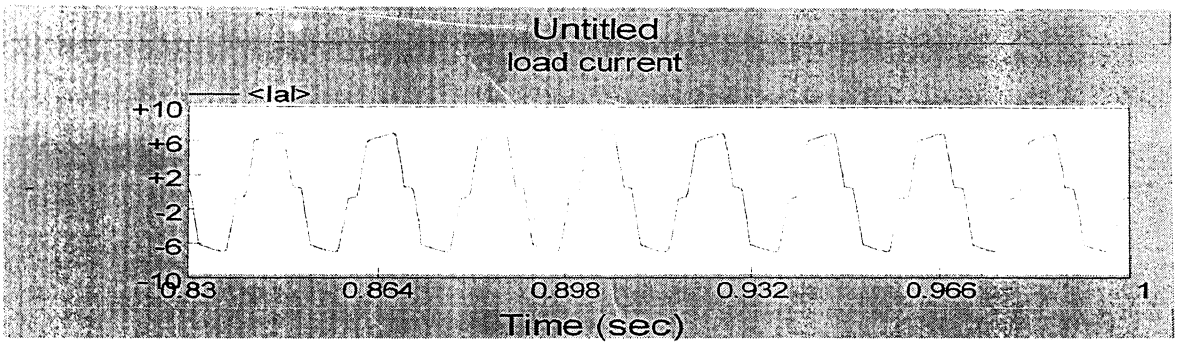


Fig. 3.12b Converter, source and load reactive power

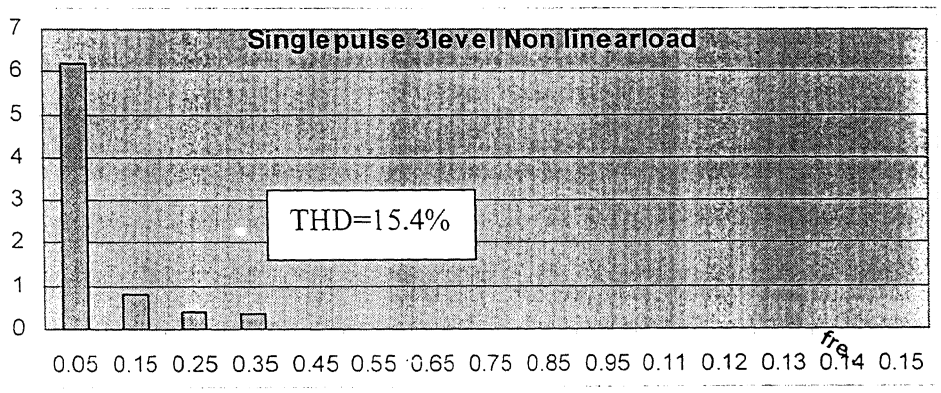


1) Single pulse based



2) Multi pulse based

Fig. 3.12.c Load current



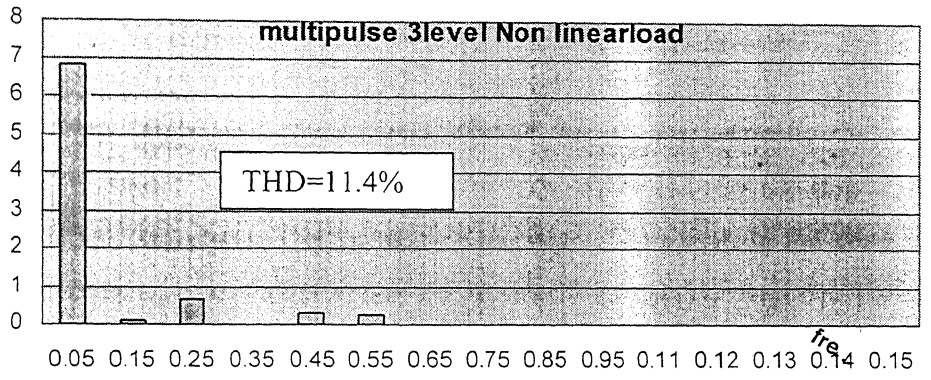
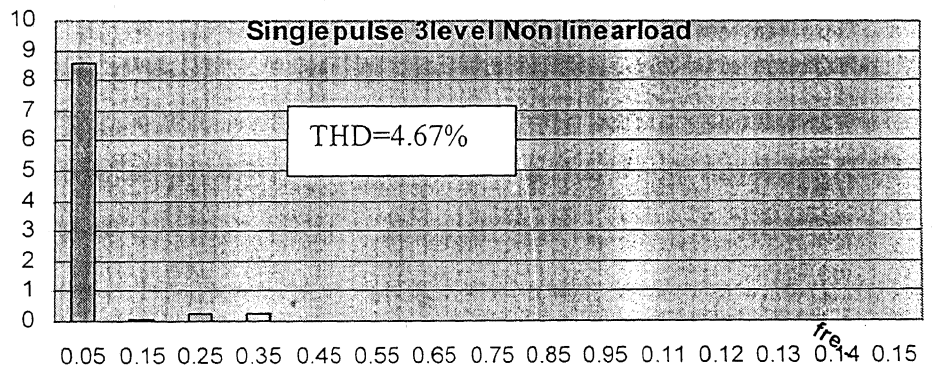


Fig. 3.13a Harmonic spectra before the auxiliary converter is made on



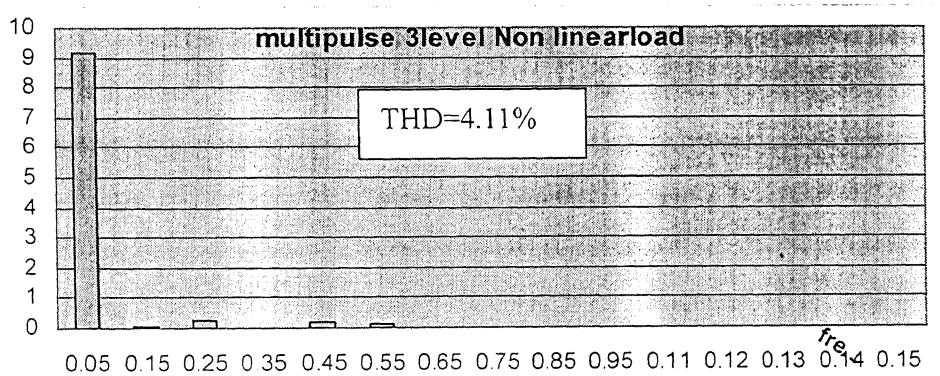


Fig. 3.13b Harmonic spectra after the auxiliary converter is made on

3.7.4 Performance Comparison

In both single pulse and multi-pulse SPWM based arrangements, the harmonics introduced is higher because of the non-linearity of the load in addition to the non-linearity of the converters. The harmonics spectrum shows that, in the absence of the auxiliary converter, even though not in the IEEE-519 acceptable range, the harmonics in case of the multi-pulse based case is much better than that of the single pulse based.

3.8 Conclusion

This chapter has presented the design and simulation aspect of a high power three level (NPC) active power filter. A parallel converter topology has been considered. The main converter is operated separately in single pulse and multi-pulse PWM and the performance is compared. The simulation result includes both linear and nonlinear load. The APF is found to be effective in compensating the load harmonic and reactive currents.

Chapter 4

Conclusion

4.1 Conclusion

The adverse effects of loads that draw high reactive power and harmonics on voltage stability and power quality make the field of active power filter an area of continued research interest. The continuous endeavors towards further improvement of existing techniques have been reviewed in the literature to emphasize this fact.

Output wave shape improvements achieved by using higher level converters is overshadowed by the control complexity and increased component count.

In this thesis, a parallel combination of high power low frequency and low power high frequency power converter arrangement (main and auxiliary converters) is used to attend the problem. Two level and three level (neutral point clamped) topologies have been considered for the main converter. Effects on both linear and non-linear loads are simulated. The main converter firing pulses are generated by a single pulse and multi-pulse SPWM techniques. A performance comparison in using the two techniques is made.

The parallel combination of high power low frequency and low power high frequency converters for reactive power compensation and harmonic elimination grants a superior performance characteristic for the system. For the high power load presented, both for two level and three level cases, the combination is shown to be useful. The THD level before and after the auxiliary converter is made on, reveals that the auxiliary converter is indispensable in eliminating the harmonics. It makes the harmonics level low so that the range specified by IEEE-519 standard is met.

A further observation at the THD level shows the significant role of the auxiliary converter in case of non-linear loads. The severe source current wave shape distortion in case of non-linear loads badly needs the back up of the auxiliary converter.

The relative improvement of the output current of the main converter in case of multi-pulse based SPWM eliminates a few selected harmonics, but it doesn't guarantee to reduce the distortion to an acceptable level with the auxiliary converter taken off.
So long as the auxiliary converter is there, both single pulse and multi-pulse based control techniques used in generating the main converter firing pulses are acceptable. The switching loss due to the relatively increased switching frequency in the multi-pulse based VSI, is believed to be manageable by the GTOs. Therefore, the choice between the two techniques is left to the implementation complexity and overall cost of the system.

4.2 Scope for Future Work

This thesis dealt with the simulation considering balanced three- phase three- wire loads. So the following are suggested as future scope of work:

1. Hardware realization of the stated topology and control techniques.
2. Application of the already stated topology and control technique for unbalanced three-phase four-wire system.

References

[1] K. Chatterjee, *Synchronous Link Converter VAR Compensators and Active Power Filters*. Ph.D. Thesis, Indian Institute of Technology, Kanpur, India, 1997.

[2] M. Basu, *Some Investigations on Unified Power Quality Conditioner.* Ph.D. Thesis, Indian Institute of Technology, Kanpur, India, 2002

[3] N. G. Hingorani and L. Gyugyi, *Understanding FACTS, Concepts and Technology of Flexible Ac Transmission System.* IEEE press, 2001.

[4] J. W. Dixon and B. T. Ooi, " Indirect Current Control of a Unity Power Factor Sinusoidal Current Boost Type Three-Phase Rectifier," IEEE Trans. on Industrial Electronics, vol. 35, pp. 508-515, Nov. 1988.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design.* John Wiley& Sons, Singapore 1989.

[6] D. A. N. Jacobson and R. W. Menzies, "Comparison of Thyristor Switched Capacitor and Voltage Source GTO Inverter Type Compensators for Single Phase Feeders," IEEE Trans. on Power Delivery, vol. 7, pp. 776-781, April 1992.

[7] K. Chatterjee, B. G. Fernandes, and G. K. Dubey, "A New High-Power Low Distortion Synchronous- Link Converter VAR Compensator," IEE proc. Electrical Power Application, vol. 146, No. 3, pp. 325-335, May 1999.

[8] P. M. Bhagwat, and V. R. Stefanovich, "Generalized Structure of a Multilevel PWM Inverter" IEEE Trans. on Industry Application", vol. IA-19, No.6, pp. 1 057- 1069, November/December 1983

[9] M. H. Rashid, *Power Electronics Hand Book.* Academic Press, 2001.

[10] L. Moran, E. Mora, R. Wallace, and J. Dixon, "Line Conditioning System with Simple Control Strategy and Fast Dynamic Response, "IEE proc. of Generation, Transmission and Distribution, vol. 142, pp. 128-134. March 1995

[11] A. Akagi, A. Nabae, and S. Atoh, "Control Strategy of Active Power Filters Using Multiple Voltage Source PWM Converters," IEEE Trans. on Industry Applications, vol. IA-22, pp. 460-465, May/June 1986.

[12] L. M. Tolbert and T. G. Habetler, " Novel-Multi Level Inverter Carrier-Based PWM Methods", IEEE- IAS 1999 Annual Meeting, pp.1424-1431, St. Louis, October 10-15 1998.

[13] B. H. Khan, S. R. Doradla, and G. K. Dubey, "A Three Phase AC-DC GTO Thyristor Converter Employing Equal Pulse Width Modulation (EPWM)," IEEE Trans. on Industry Applications, vol. 27 No. 2, pp 370-379, March/April 1991.

[14] Seshagiri, R. Doradla, C. Nagamani, and S. Sanyal, "A Sinusoidal Pulse Width Modulated Three Phase AC to DC Converter-Fed DC Motor Drive," IEEE Trans. on Industrial Application, vol.IA-21, No. 6, pp. 1393-1408, Nov./December 1995.

[15] S. Dong, W. Zhonghong, J. Y. Chen, and Y. H. "Harmonic Resonance Phenomena in STATCOM and Relationship to Parameters Selection of Passive Components," IEEE Trans. on Power Delivery, vol. 16, No. 1, pp. 46-52, January 2001.

[16] J. Zubek, A. Abbondanti, C. J. Norbby, " Pulse Width Modulated Inverter Motor Drives with Improved Modulation," IEEE Trans. on Industry Applications, vol. IA-11, No. 6, November/December1975.

[17] G. Carrara, S. Gardella, M. Marchesoni, R. salutary, and G. Scitto," A New Multilevel PWM Method: A Theoretical Analysis," IEEE Trnas. on Power Electronics, vol.7, No.3, pp. 497-505, July1992

[18] A. Nabae, I. Takahashi, and H. Akagi, " A New Neutral–Point Clamped PWM Inverter," IEEE Trans. on Industry Applications, vol. IA-17, No. 5, pp. 518-522, September/ October 1981.